Architectural choices & design-implementation methodologies for exploiting extended FD-SOI DVFS & body-bias capabilities

David JACQUET

Senior Principal Engineer
CPU & GPU subsystems
Technology R&D
STMicroelectronics

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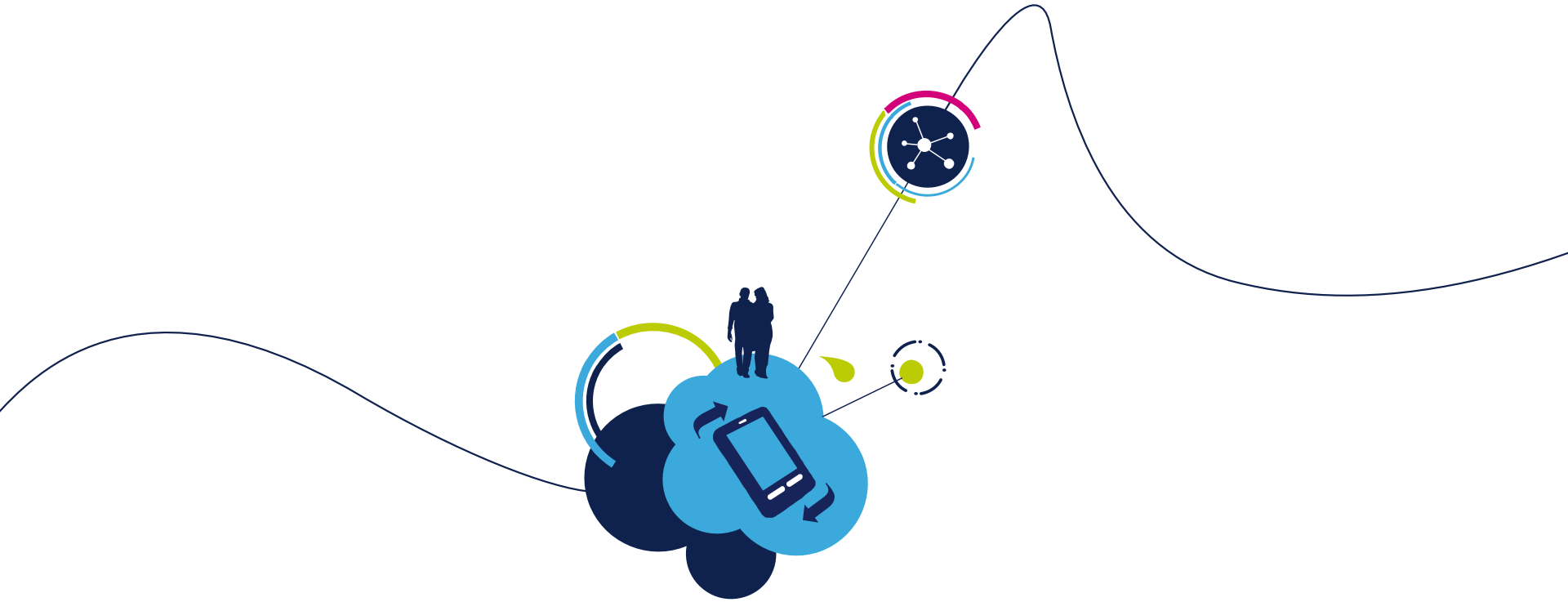
Outline

- How to increase the energy efficiency of SOCs & CPUs ?
- UTBB FD-SOI
- Total power and body biasing
- FD-SOI and multiprocessing
- Conclusion



How to increase the energy efficiency of SOCs & CPUs ?

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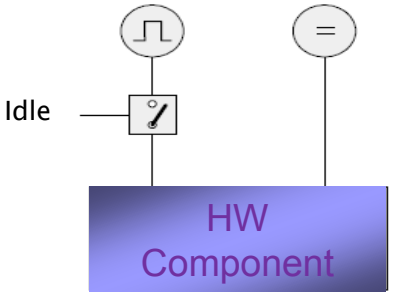
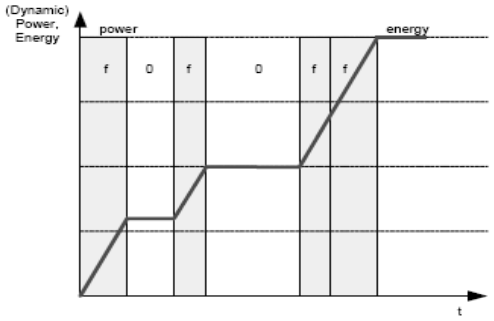
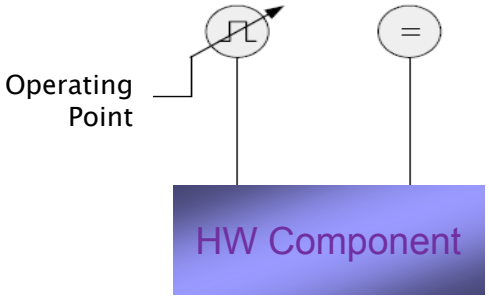
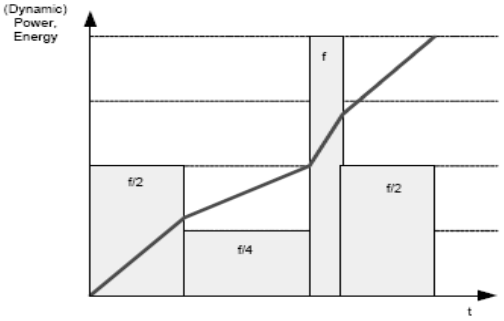
Dynamic power reduction : *from clock switching to DVFS*



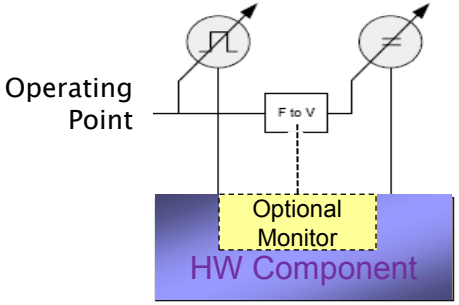


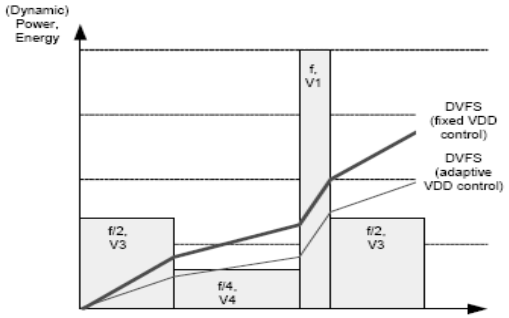
A) Clock Switching





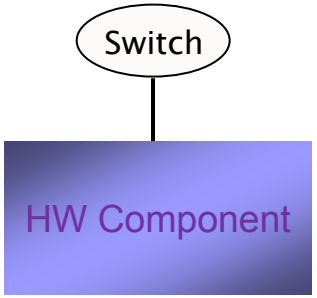
B) Frequency Scaling



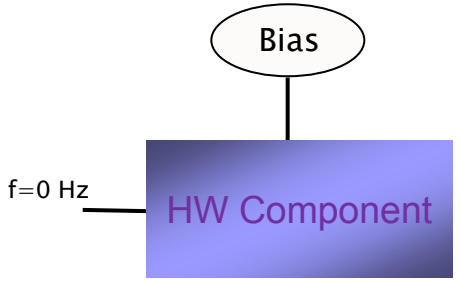


C) Dynamic Voltage Frequency Scaling DVFS

static power reduction :

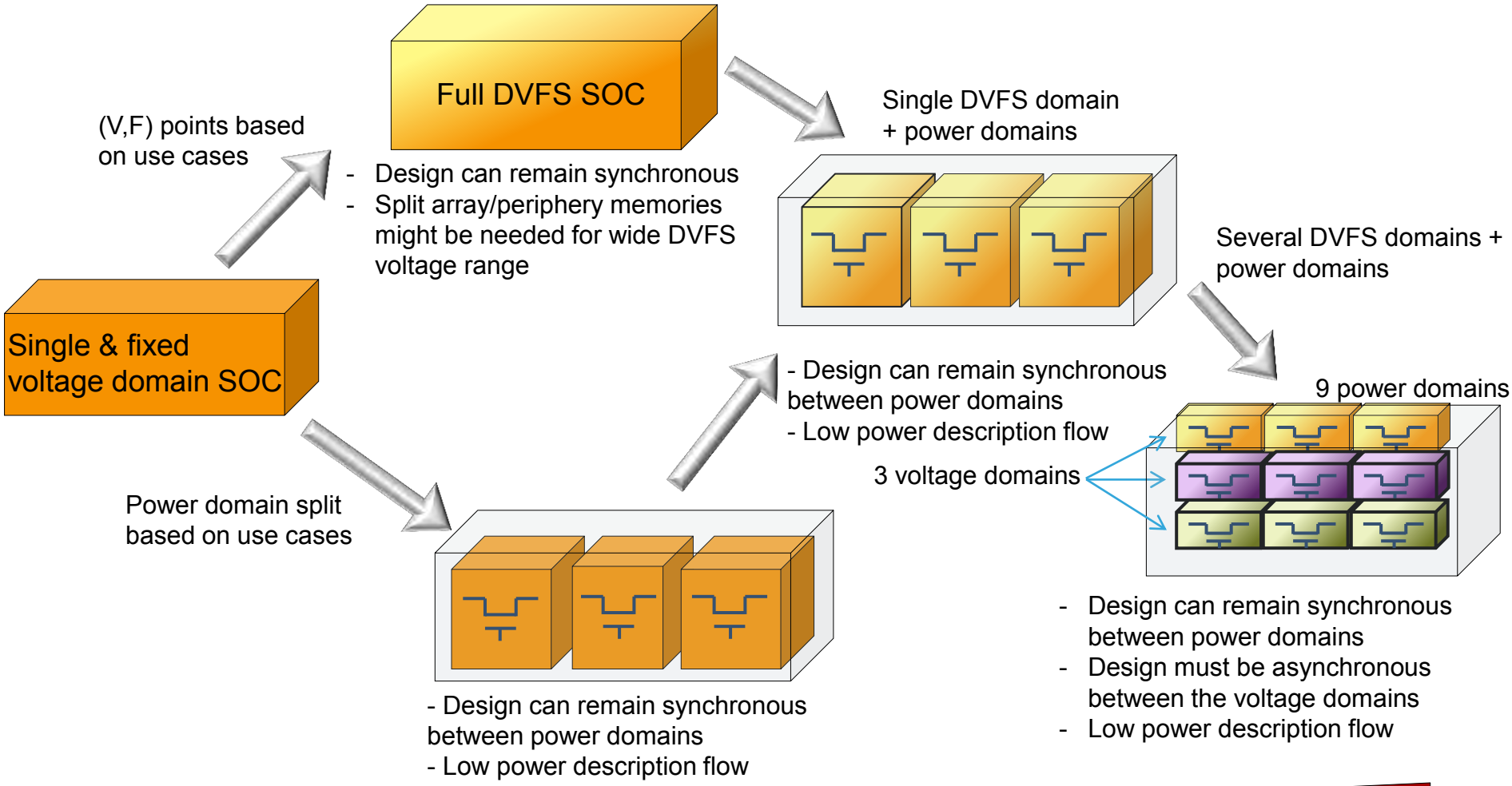


Power Gating



Retention mode

Increasing the Energy Efficiency of a SOC Architecture



DVFS, multi-voltage, multi-power domain SOC

To make	I need	System consequences
Communications between voltage domains	Level shifters Asynchronous communications - Async FIFO on buses - Signal level async protocol	- Extra latency on communications versus fully synchronous communications
Power domains	Power switches	- For each power domain, an individual management of clock, reset and isolation is mandatory
Voltage domains	External Independant voltage sources	- Several voltage sources with a control link from the SOC
DVFS on a voltage domain	Variable voltage source	- PLL control per DVFS domain - Link between the SOC and the external voltage source - Split array/periphery memories if the DVFS voltage must be lower than bitcell min voltage

How to increase the energy efficiency of computing systems ?

- Several techniques exists but bulk process limits their efficiency at advanced process nodes (28/14 nm)

Technique	Limitations in Bulk
Increasing the # of processing cores	• leakage current for a given performance • see “Wide range DVFS limitations”
Poly biasing of the transistors	• limited gate length modulation range
Wide range DVFS	• [Vmin, Vmax] range is limited by variability • Huge performance degradation when supply V reduces • dual rail memories limited Array/periphery voltage gap • Memory Array minimum voltage
Dynamic transistor Vt control	• limited body bias range (-300 mV, +300 mV) • limited benefit in 28 nm & almost no benefit in 20/14 nm

- A new process & design techniques are needed

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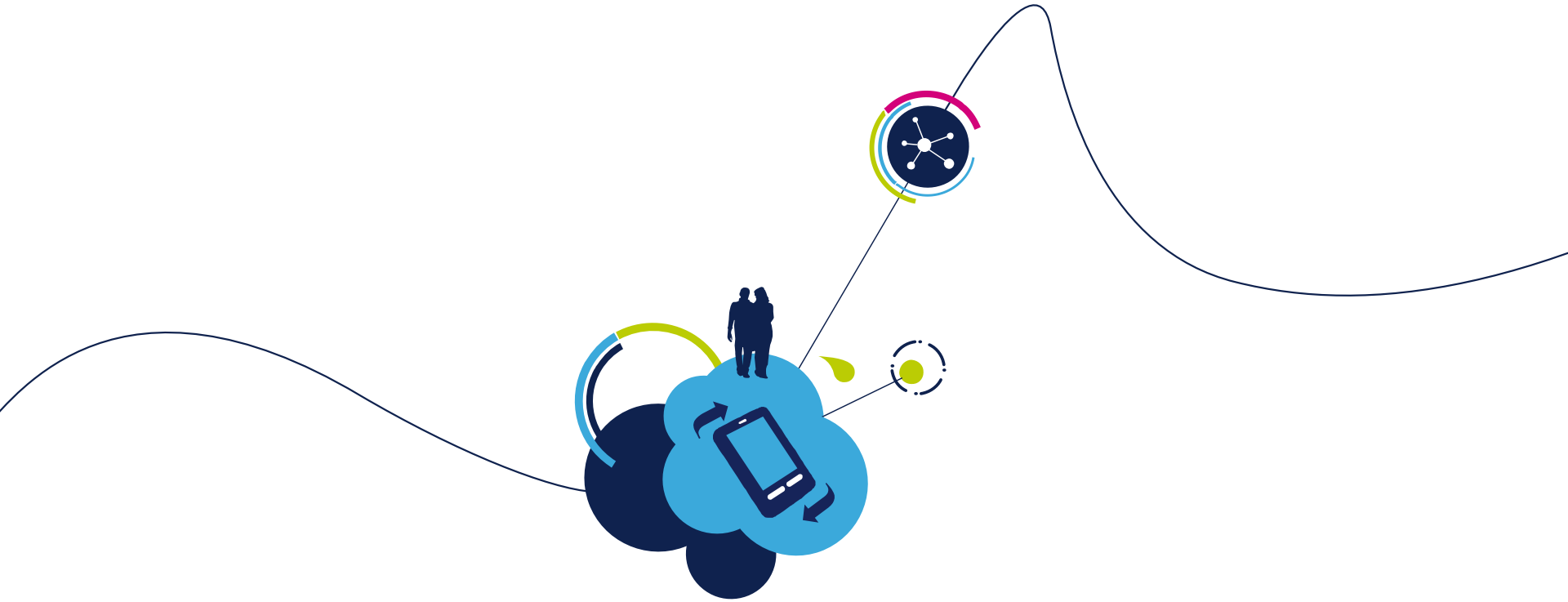

UTBB FD-SOI

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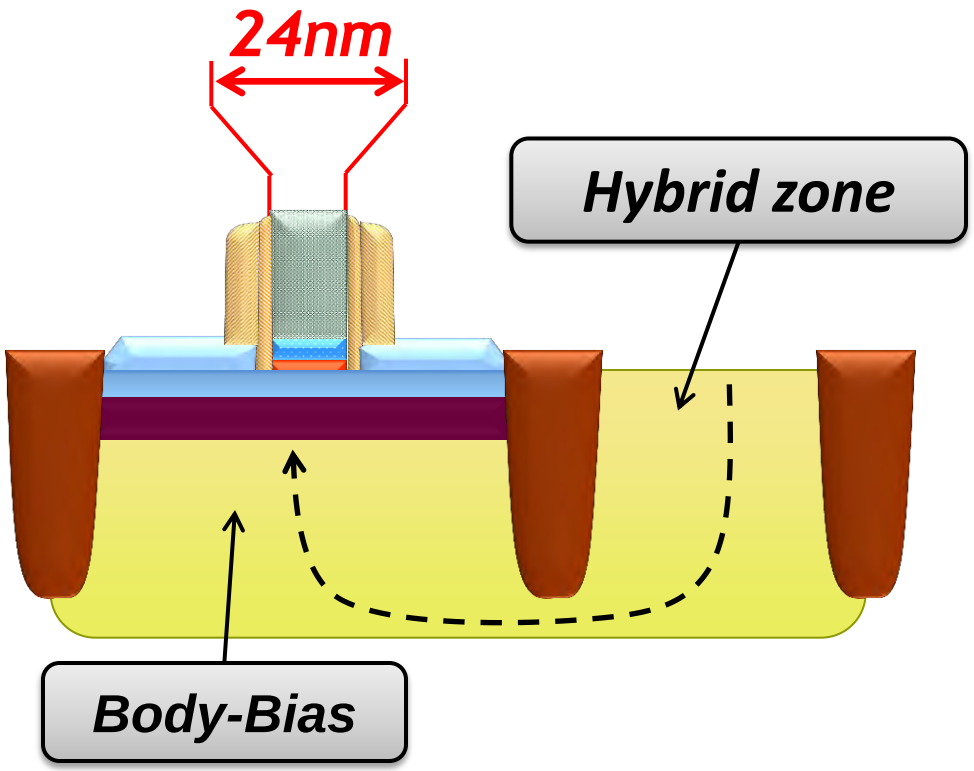
28nm Planar UTBB FD-SOI: Advantages

UTBB FD-SOI enables shorter channel length



- **Ultra-thin body**
  - Better SCE immunity
- **Ultra-thin BOX**
  - Extended body biasing
- **Total dielectric isolation**
  - Latch up immunity
- **No channel doping**
  - Improved variability

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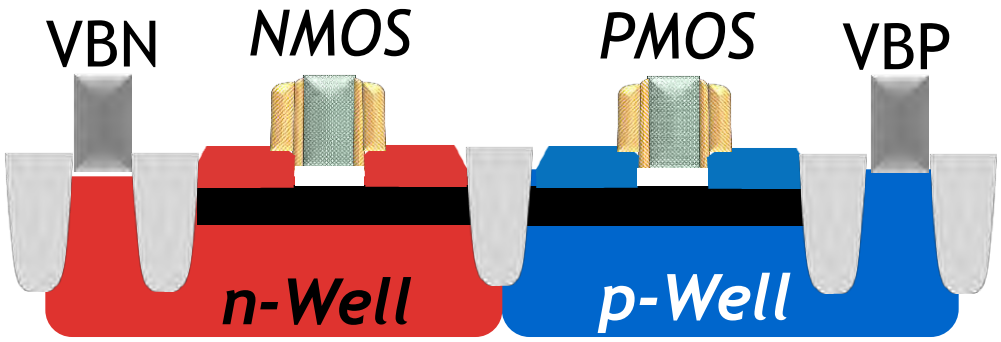
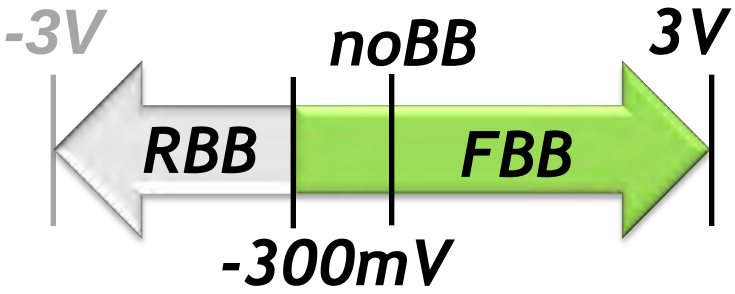
UTBB FD-SOI: Extended Body Voltage Range

- **Flip Well for full forward body-bias operation**





Unique feature for dynamic speed/leakage optimization

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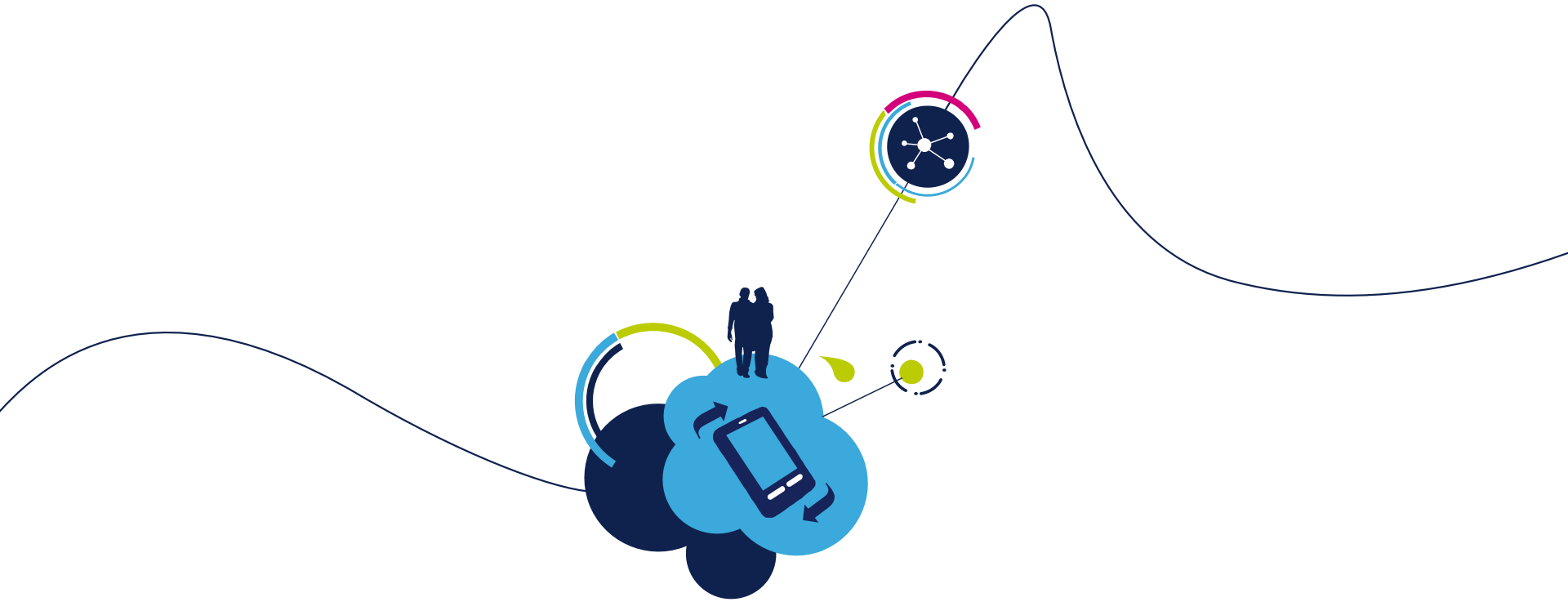

The total power & body biasing

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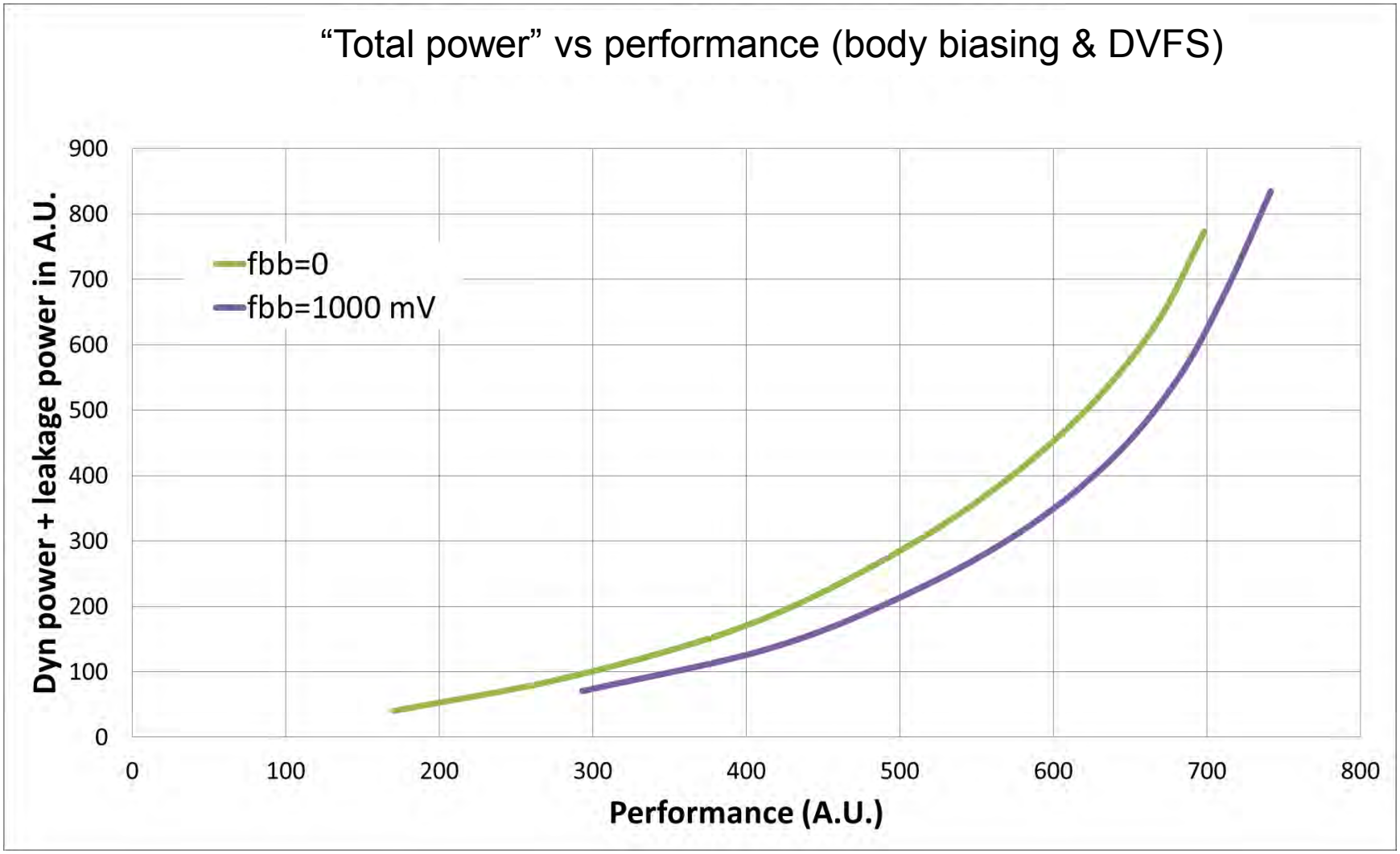
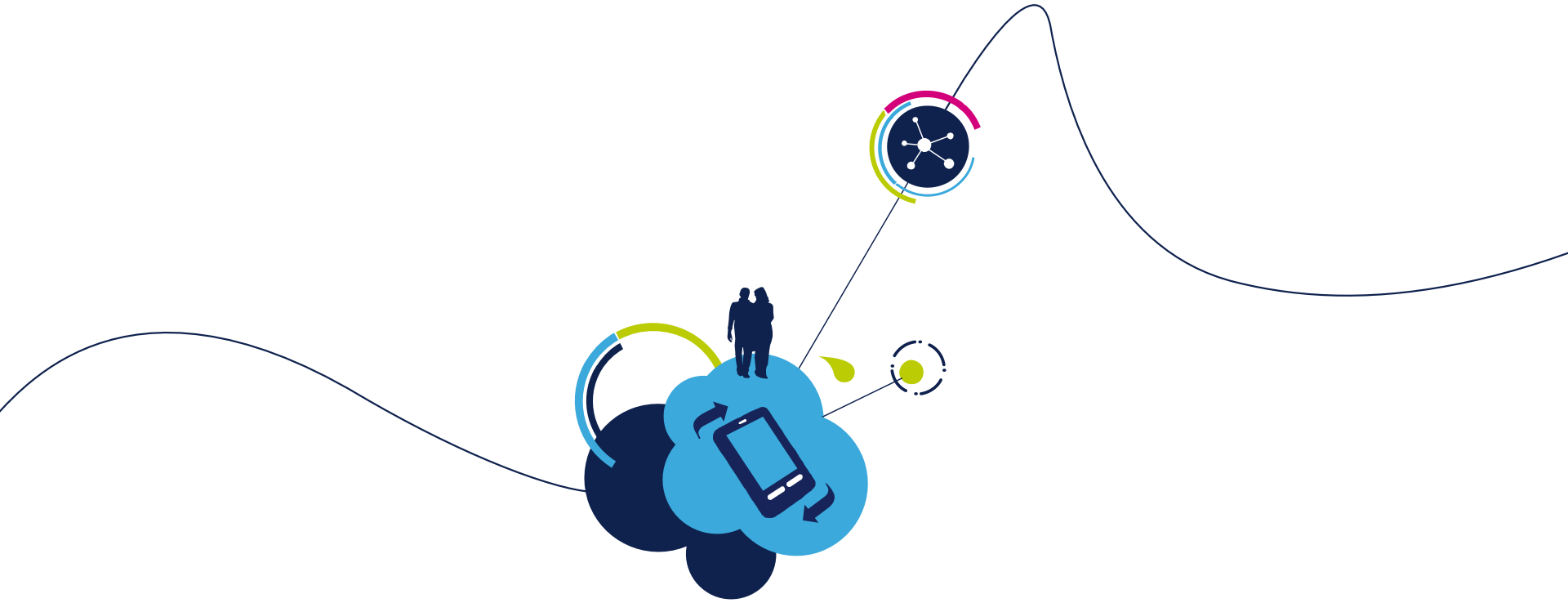
Energy Efficiency and Leakage

- In any technology node, a tradeoff must be made between speed and leakage
  - At a given voltage
    - The maximum speed can be increased at the expense of higher leakage
  - Or for a given maximum speed
    - The minimum voltage to reach this performance can be reduced at the expense of higher leakage
    - The lower the supply voltage, the lower the dynamic power (in ~V^2)
  - At the end, what counts is the “total power”=leakage+dynamic power
- In FD-SOI, the wide Body-Bias range allows this tradeoff to be dynamically optimized to the conditions
  - Process conditions
  - Temperature conditions

Total power graph example – 28nm FD-SOI





Dual ARM A9 in 28nm FD-SOI

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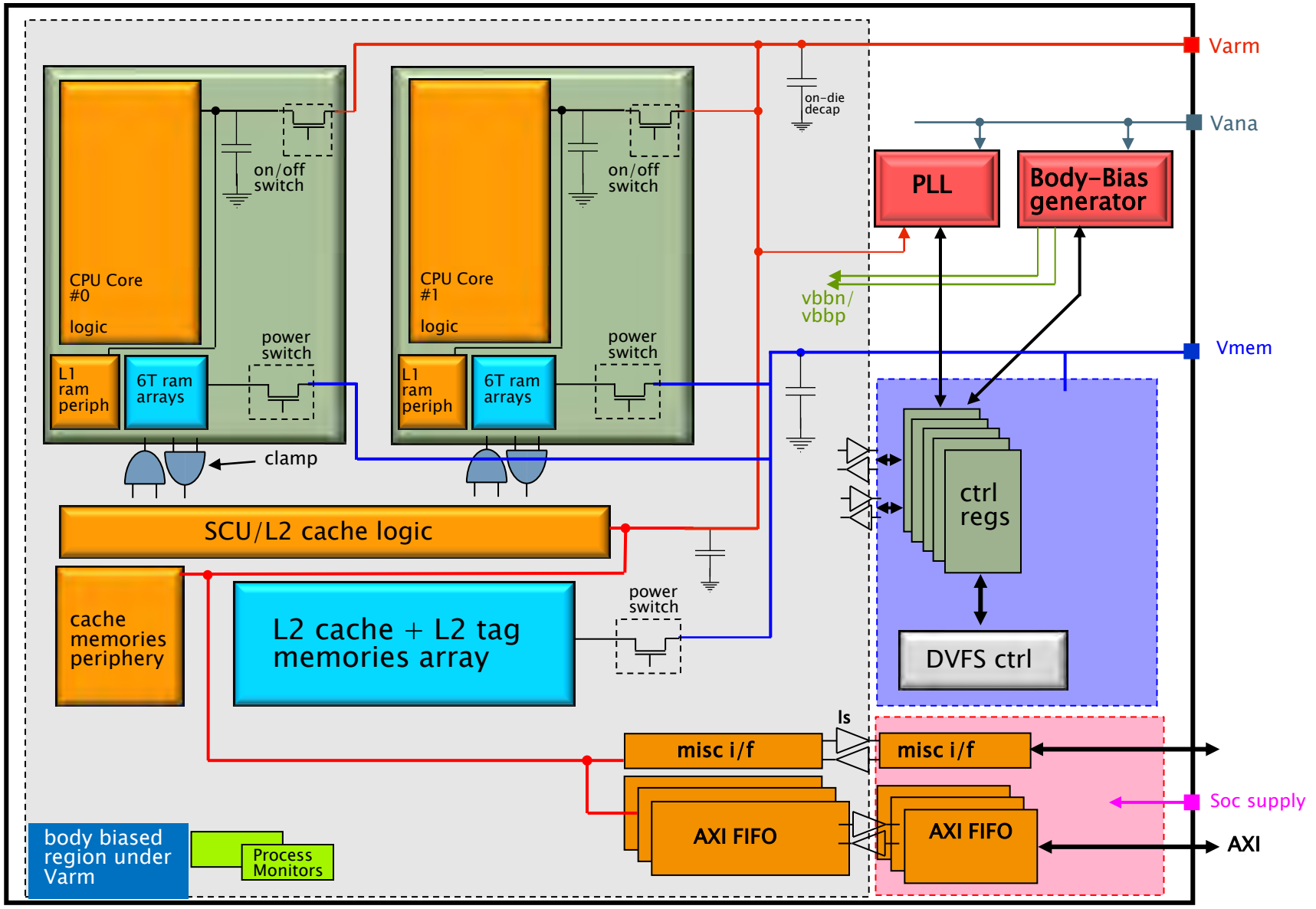
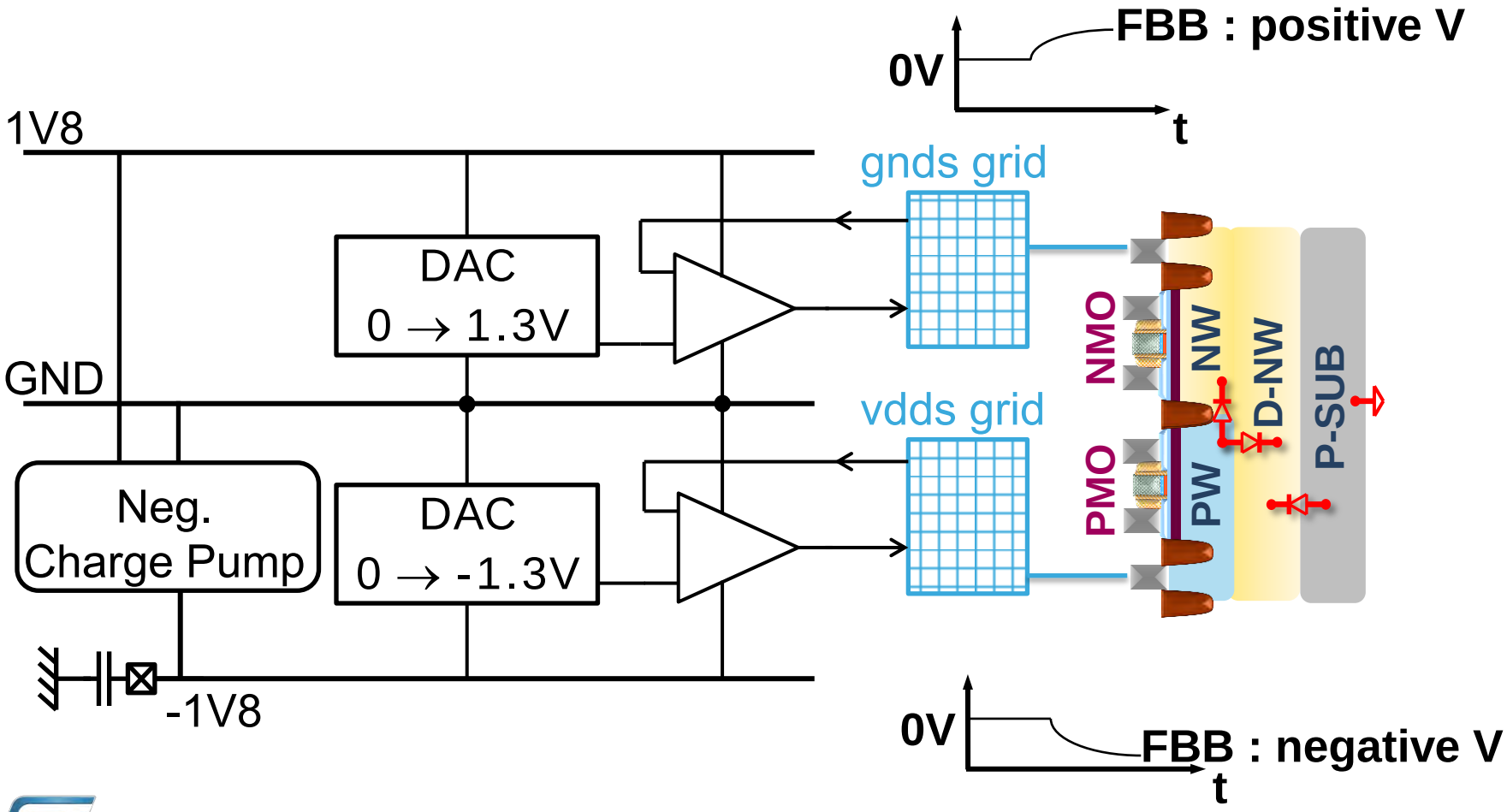
Dual ARM A9 subsystem architecture



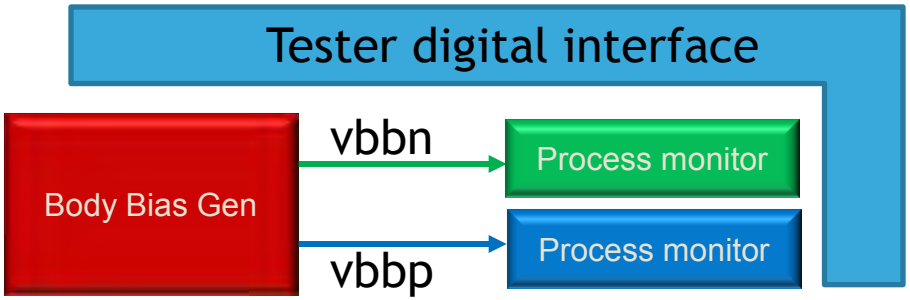
Body-Bias voltage generation

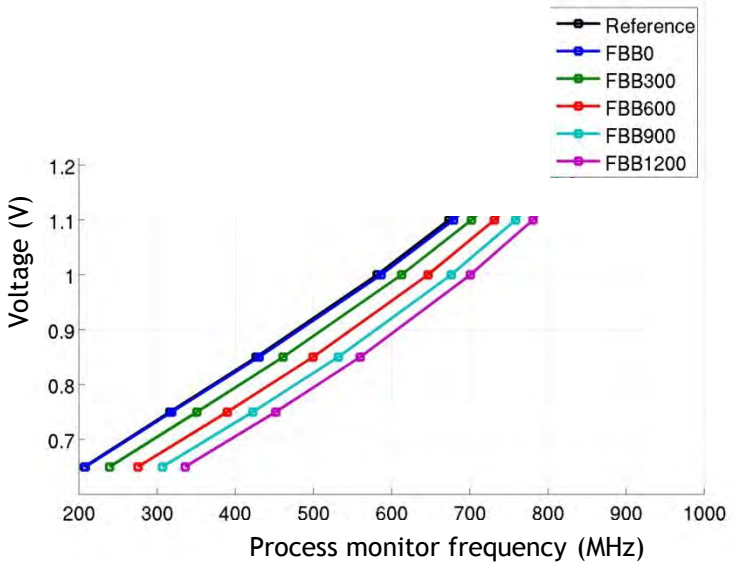
- How to generate programmable body voltages ?



Fully digital testing of the BBgen

- The BBgen is generating 2 independent voltages
  - For the Nmos [0 to 1.3V] & Pmos [-1.3V to 0V] bodies
  - With a resolution of 100 mV
  - The embedded process monitors allow a full digital test of the BBGen in production test
    - No need for body nodes external access
    - Full access via a digital interface





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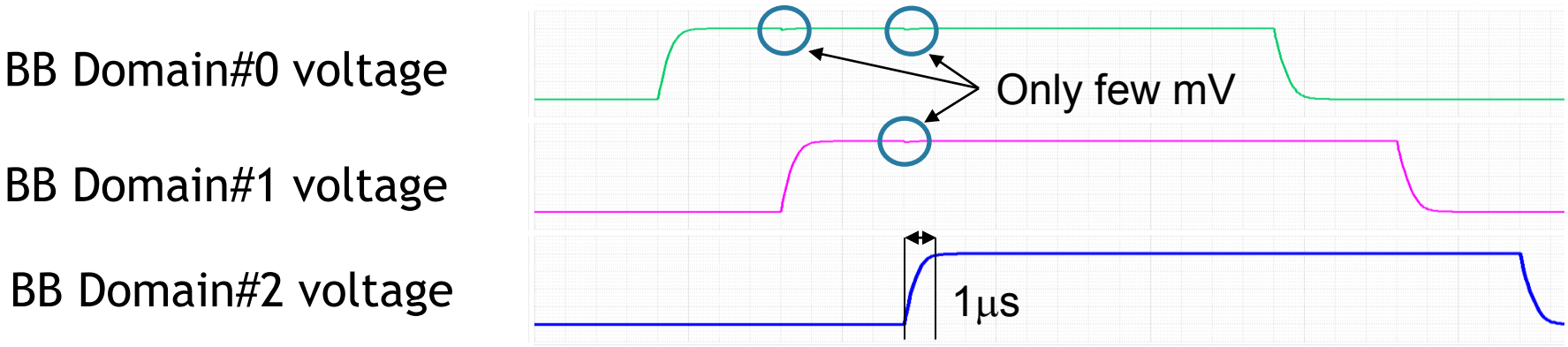
Fast dynamic body-bias management

- Low Z_{out} amplifiers allow μs settling time of the body nodes
  - E.g. 3 body domains connected to the same generator
  - Each body domain can be activated
    - In less than 1μs
    - Activating any body domain does not disturb the voltage of the others



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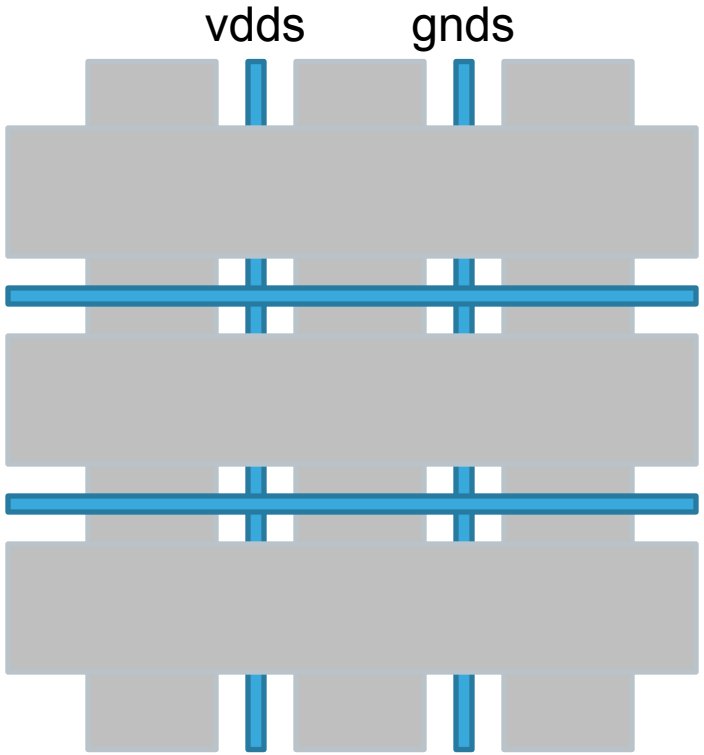
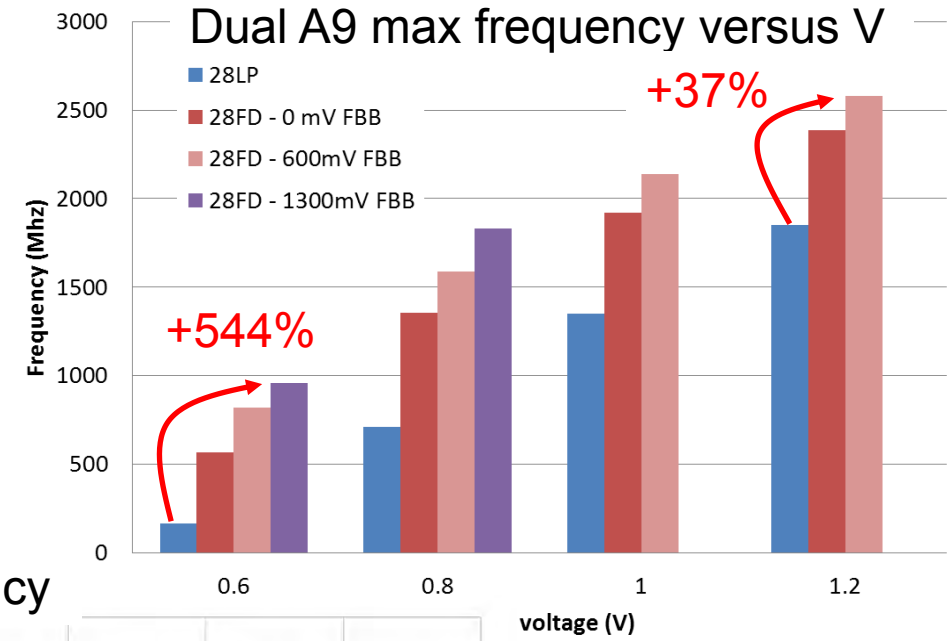
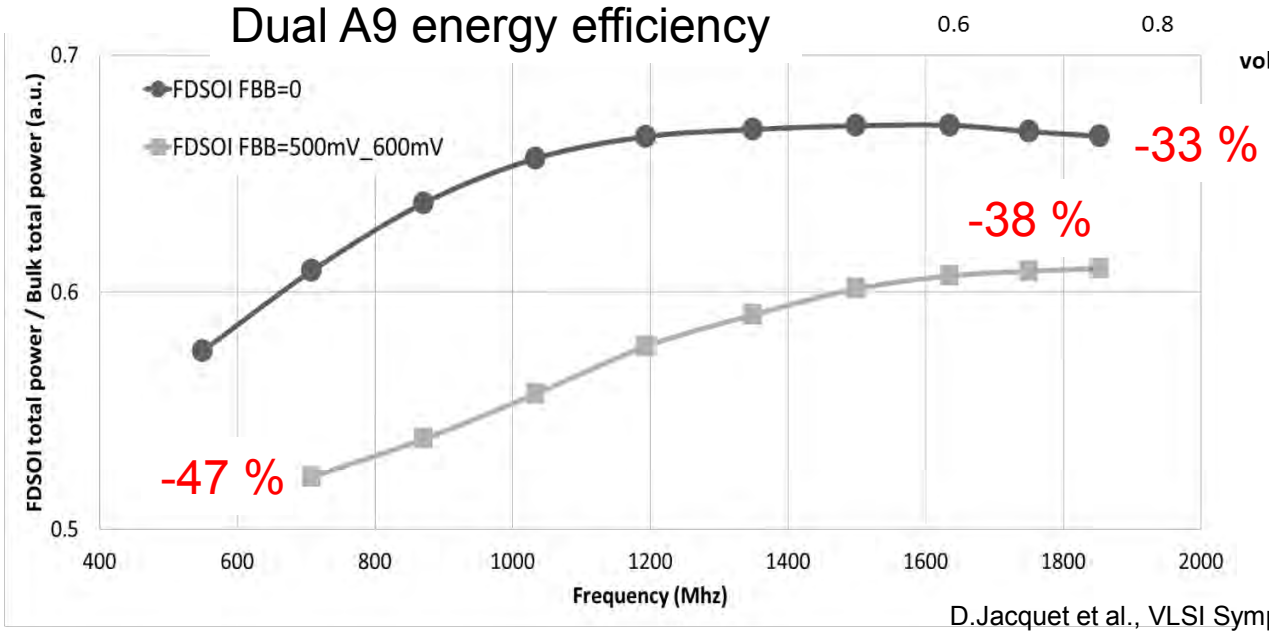
Body-Bias voltage grid

- A very thin [X,Y] grid is routed over the body-biased region
  - No static current has to be provided
  - The current is limited to “C.dV/dt” during the body-bias transitions



28FD Dual A9 Energy efficiency





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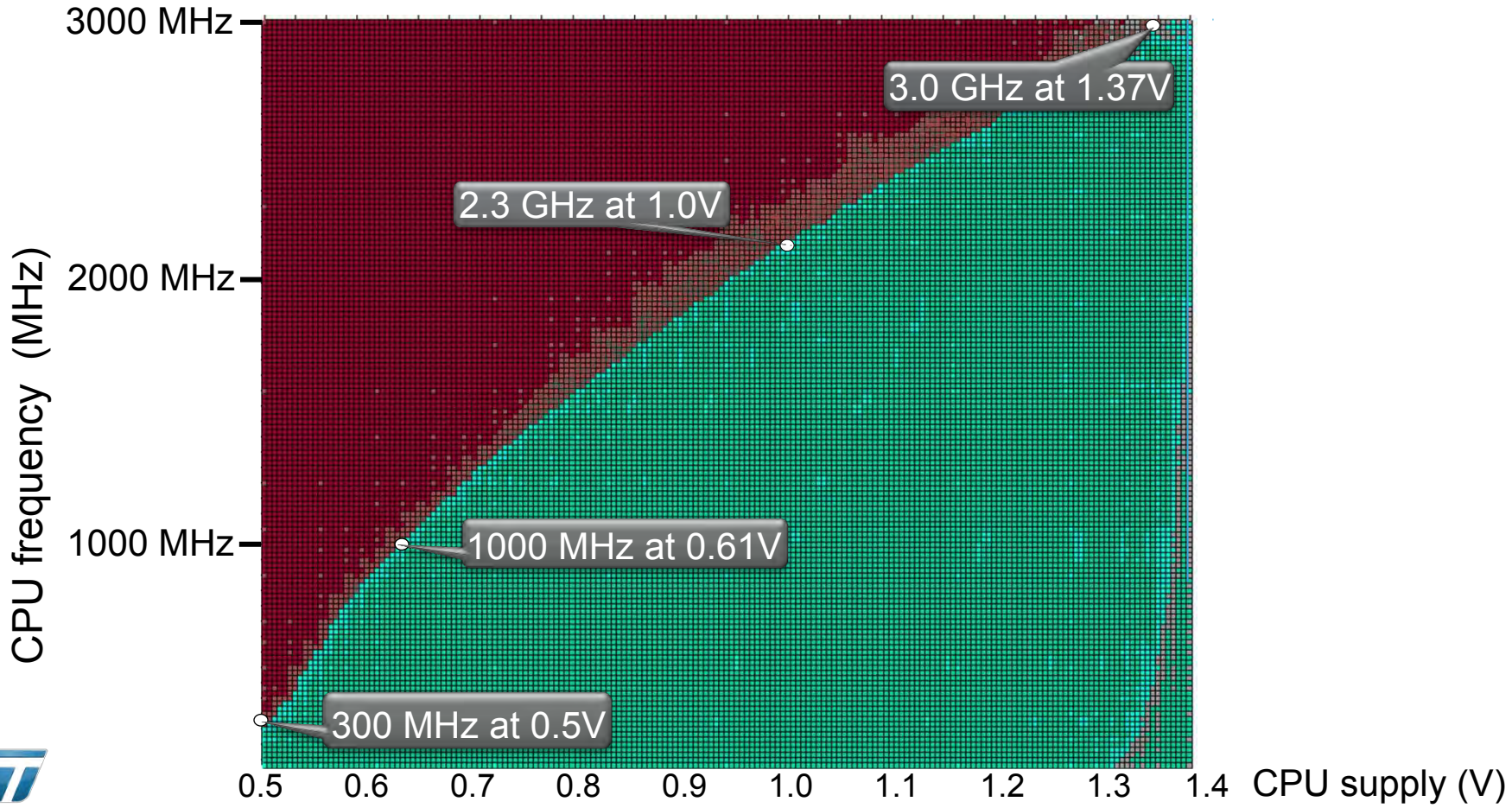
Continuous & wide DVFS

- 0.5V to 1.4V DVFS range
- Continuous functionality in this voltage range



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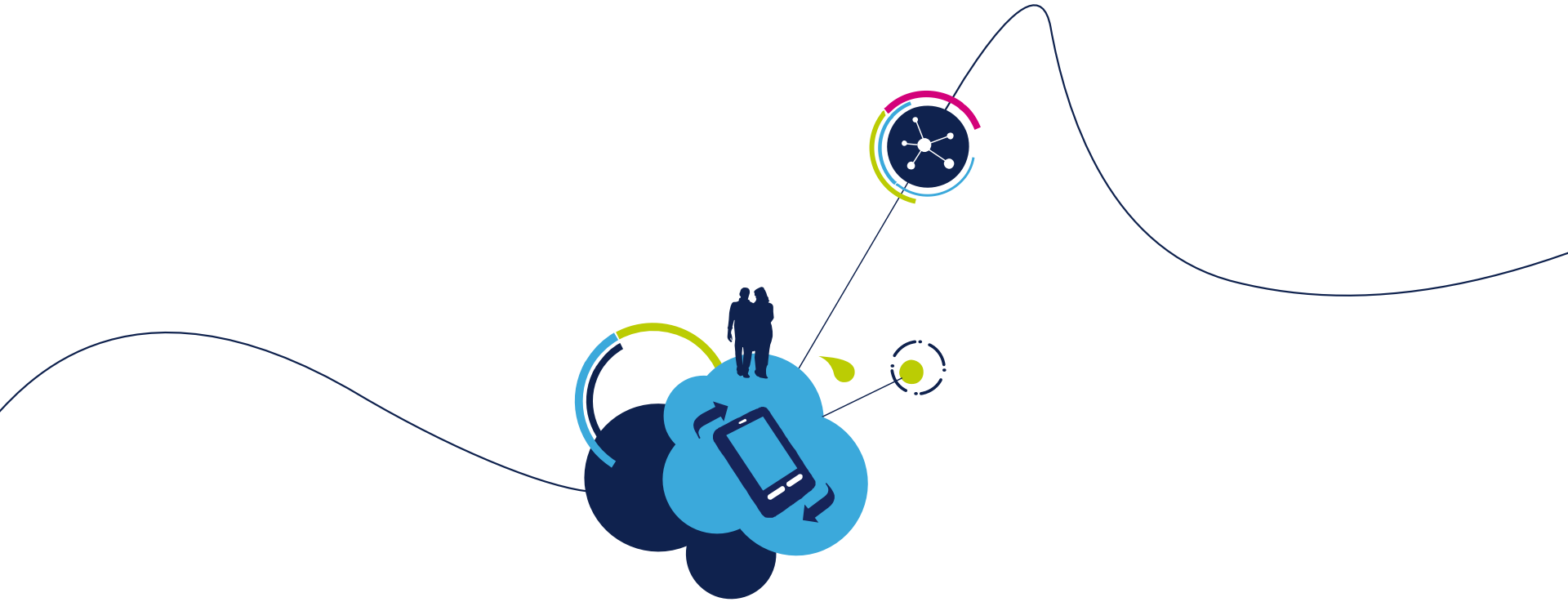
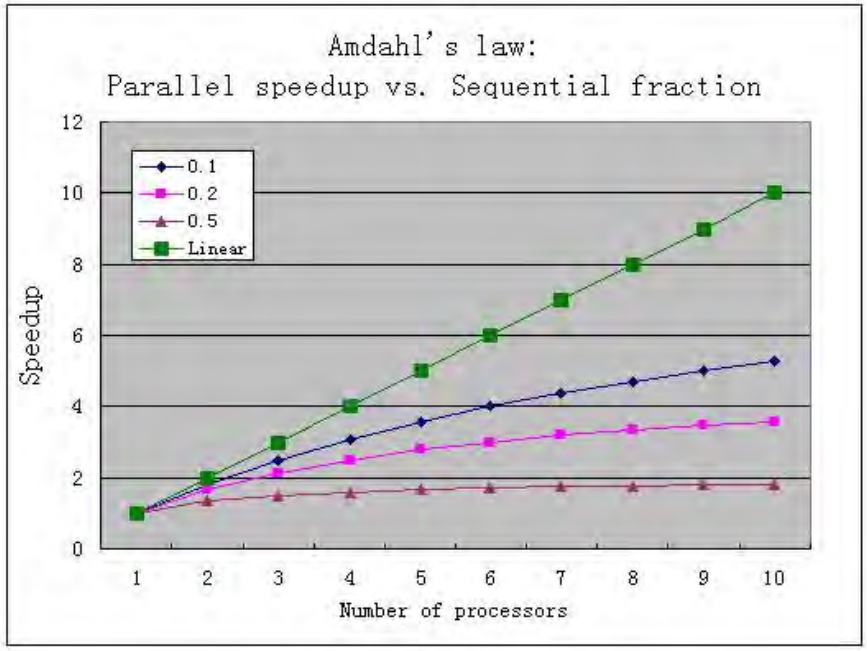


FD-SOI & multiprocessing

Multicore Delivers more MIPS/mW

- No doubt multicore can deliver more MIPS per mW
  - Core should be implemented for best power efficiency/peak frequency trade-off
  - SoC should host as many cores as possible at every technology node
    - scalability achieved through core number increase
    - no more by frequency scaling
- Major issues
  - Amdahl's law
  - Memory hierarchy efficiency



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Multiprocessing and wide DVFS - 1

- FD-SOI provides more performance at same voltage as bulk
- Also a much lower performance degradation when lowering the supply voltage (dperf/dV)
- And, as consequence, a very good efficiency on multiprocessing applications

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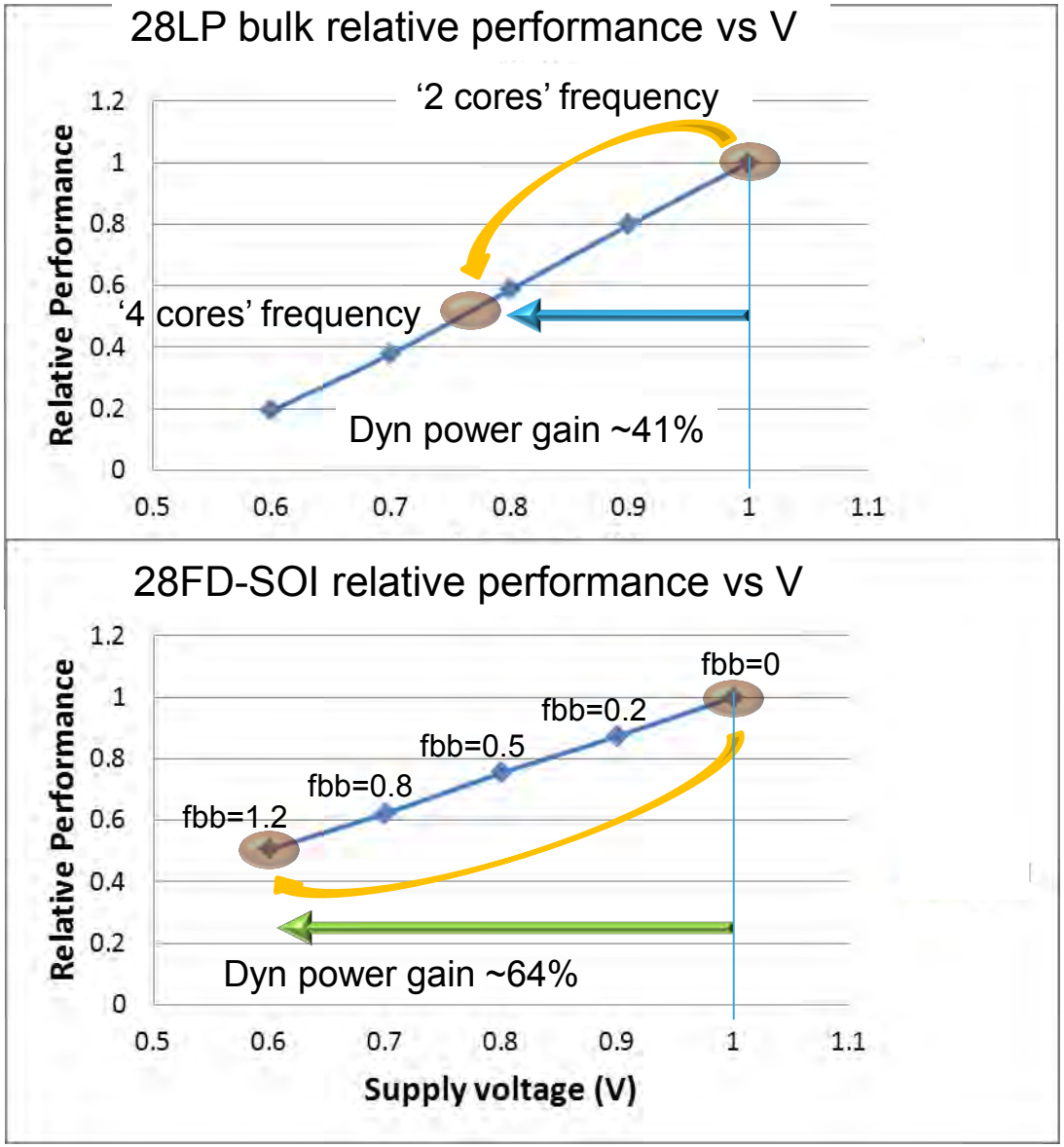
Multiprocessing and wide DVFS - 2

- 2 cores vs 4 cores
  - Ideal speed up factor
  - 2 cores@F=4 cores@F/2



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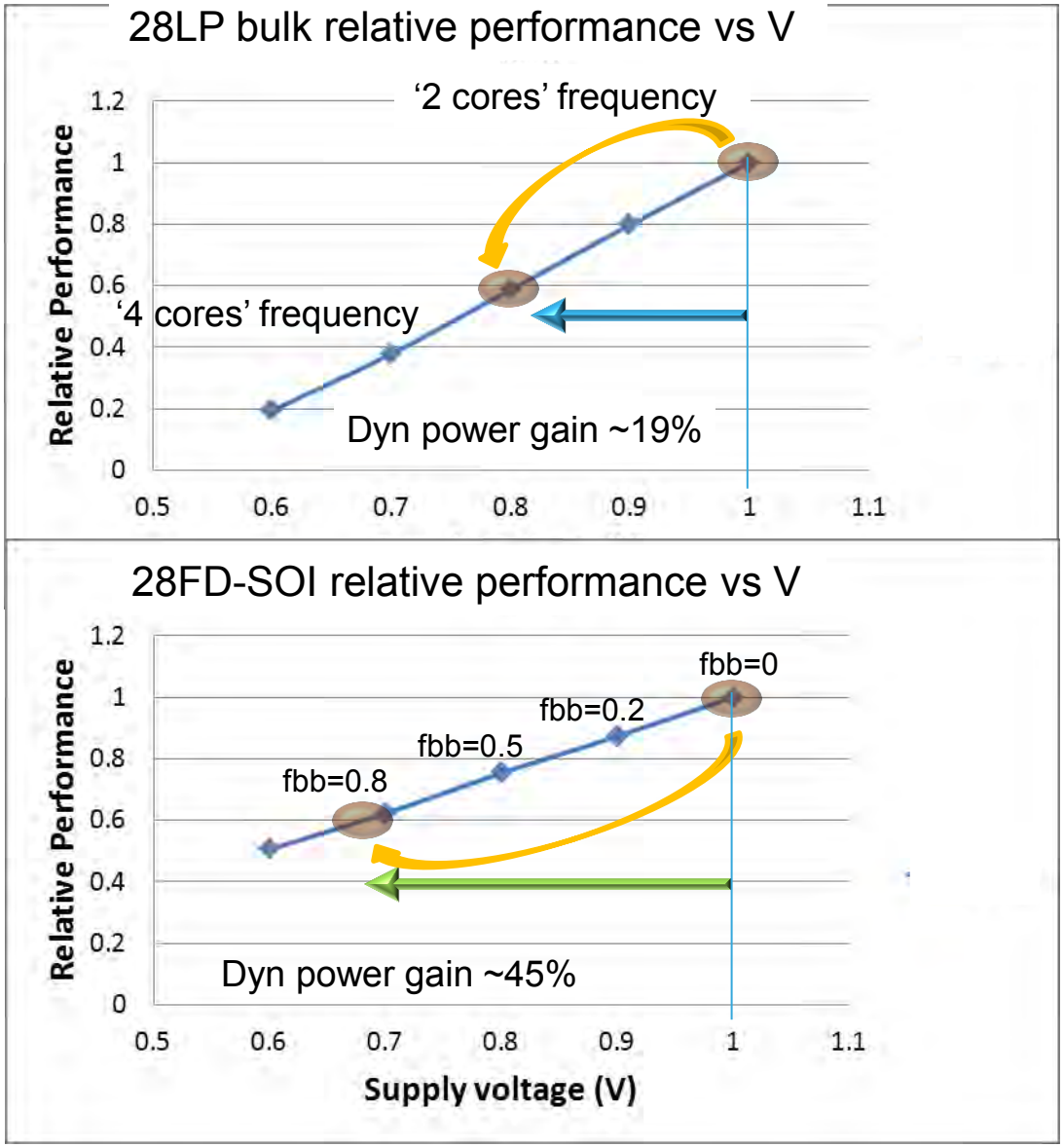
Multiprocessing and wide DVFS - 3

- 2 cores vs 4 cores
  - Seq fraction = 0.1
  - 2 cores@F=4 cores@0.6F



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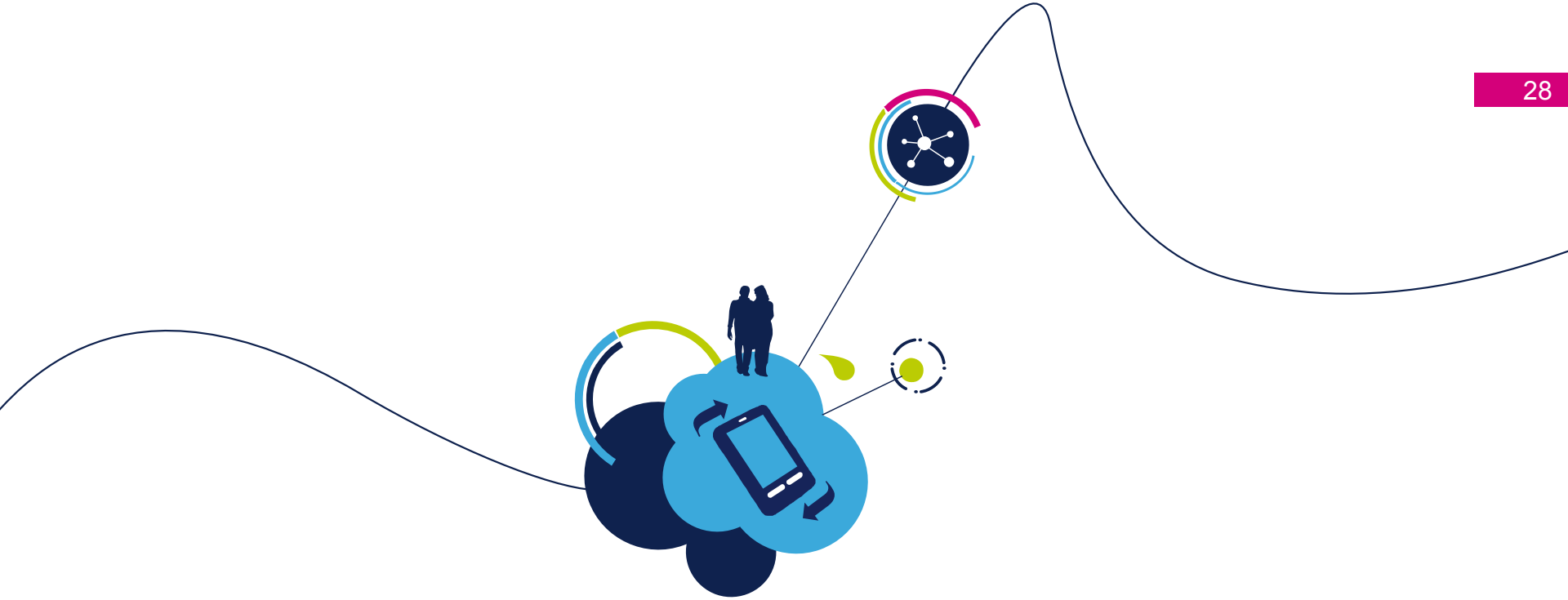
Conclusion

- We have demonstrated that FD-SOI enables dynamic management of the leakage/dynamic-power tradeoff
- The Energy Efficiency of Multiprocessing systems can be perfectly exploited thanks to FD-SOI high performance at low voltage & wide DVFS range
- A first-time silicon success Dual ARM A9 in 28nm UTBB FD-SOI demonstrates
  - CPUs running from 300 Mhz@0.5V to 3000 Mhz in continuous DVFS
  - Fully integrated
    - Body-Bias generator
    - Advanced IPs for power management



Thank You