

Teaching module IP : From Design to TEST

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Panel on new developments @ CMP

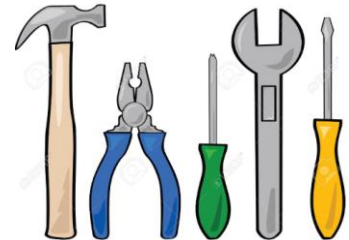
Date : 30/01/2020

Teaching module IP : From Design to TEST

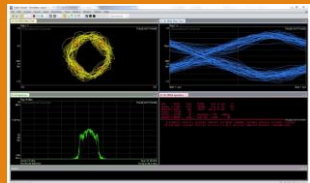
Share our experience



Propose some tools for teachers



1st Year (2nd year of Engineering School)



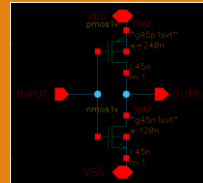
System Study

- 12 Hours
- Matlab and ADS



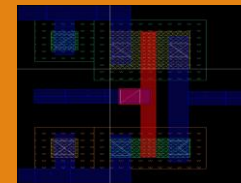
Project Management Case study

- Team organization
- Work flow definition



Schematic level design

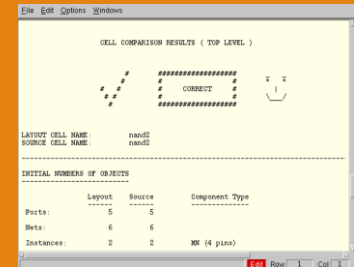
- 40 Hours
- Virtuoso



Layout design

- 40 Hours
- Virtuoso

Deliverable



DRC and LVS clean GDS

2nd Year (3rd year of Engineering School)

Based on
Student's IPs
and
Back-up IPs

4
Practical
Training

PA measurement (NL - VNA)

PLL measurement (SA, Phase-Noise)

LNA measurement (Noise – VNA - SA)

System measurement (89600-Modulation, ACPR ...)

What we propose

Propose a framework to the academic community to teach RFIC

Students

- learn how to design IC
- provide GDS for a tapout
- measure their own circuits

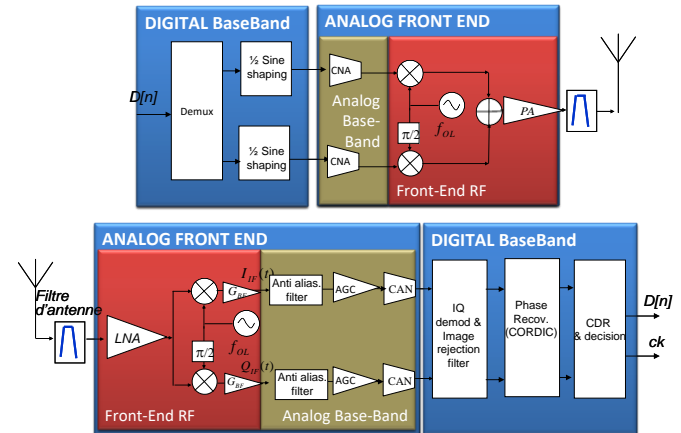
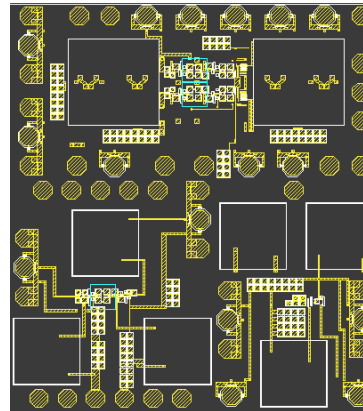
Teachers

- PHELMA/CMP provide reference design (IP)
- PHELMA/CMP provide design and measurement tutorials
- Access to MPW with CMP

What we propose

Reference Design: ZigBee Transceiver Building Blocs

- PA
- TX (IQ Mix + PA)
- RX (LNA + Mix)
- LNA
- PLL

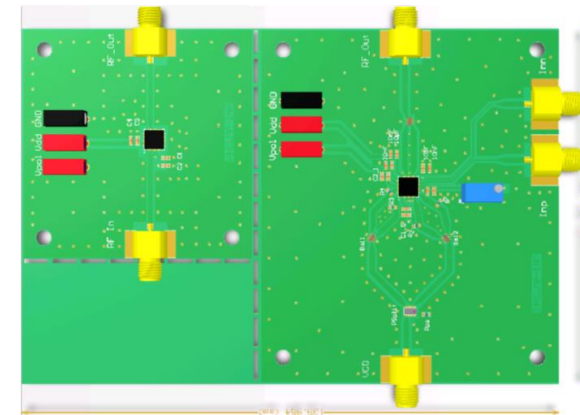


The Technology

- AMS 035 (BiCMOS)

Eval Bords :

- 2 ports eval board (LNA / PLL / PA)
- 4 Port eval boars (TX-RX)



Design Tutorials

- Transciever System study
- LNA
- PA
- PLL
- Gillbet Cell

Measurement Tutorial

- VNA based linearities measurements (PA)
- 89600 based modulation measurements (TX or RX)
- PLL measurements
- VNA based SP measurements

THANK YOU

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