SOIMUMPS surface micromachining technology

Overview

CMP distribute the SOIMUMPS technology from MEMSCAP. The technology process uses deep Reactive Ion Etching steps on a Silicon On Insulator wafer.
Figure 1 shows arrangements of different layers.

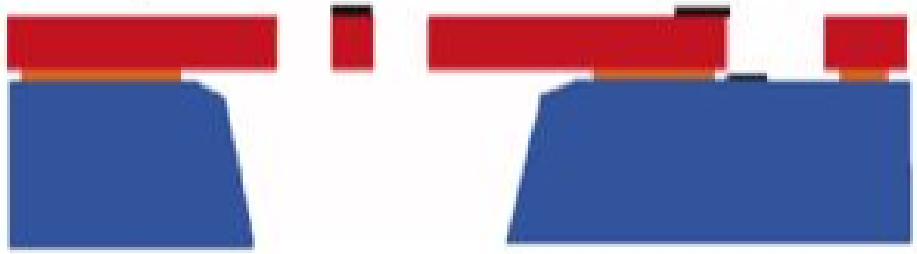

Figure 1: cross section view of the SOIMUMPS surface micromachining technology

Design

Design handbook, techno files and DRC files are available upon request.

Fabrications

Die sites are fixed size and no additional post process are required.

Application

Examples of SOIMUMPS applications are available on MEMSCAP web site.

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