MEMS Prototyping

SOIMUMPs:
Silicon-On-Insulator
Multi User MEMS Processes

www.memscap.com
www.memsrus.com

The Multi-User MEMS Processes, or MUMPs®, is a commercial program that provides cost-effective, proof-of-concept MEMS fabrication to industry, universities, and government worldwide. Within the MUMPs® program, MEMSCAP offers three standard processes: traditional PolyMUMPs, MetalMUMPs, and SOIMUMPs.

Inspired by the tremendous success of the polysilicon surface micromachining PolyMUMPs process, which has delivered hundreds of thousands of MEMS chips to users over nearly a decade and 50 wafer runs, MEMSCAP introduced a new multi-user process focused on building SOI MEMS devices in late 2002.

The Silicon-On-Insulator Multi User MEMS Processes, or SOIMUMPs is a MEMS micromachining platform that allows the user to build MEMS devices in SOI using a standard set of design rules. The advantages to the user community of such a standardized platform have already been demonstrated both in PolyMUMPs and in other semiconductor processes such as CMOS fabrication. The process itself is standardized and run repetitively resulting in a robust, manufacturable process platform. Design rules are well defined so design outcomes are predictable. Entry costs are low because of the shared-wafer-cost environment; transition from prototype to manufacturing is virtually seamless since the process

KEY PROCESS FEATURES

(1) A silicon-on-insulator (SOI) wafer is used as the starting substrate, with the following layer thicknesses:
•Silicon thickness:10 ± 1 μm
•Oxide thickness:1 ± 0.05 μm
•Handle wafer (Substrate) thickness:400 ± 5 μm

(2) The Silicon layer is patterned and etched down to the Oxide layer. This layer can be used for mechanical structures, resistor structures, and/or electrical routing.

(3) The Substrate can be patterned and etched from the “bottom” side to the Oxide layer. This allows for through-hole structures.

(4) A shadow-masked metal process is used to provide coarse Metal features such as bond pads, electrical routing, and optical mirror surfaces.

The SOIMUMPs Process

The SOIMUMPs process is a simple 3-mask level SOI patterning and etching process derived from work performed at MEMSCAP. This process flow was originally developed for the fabrication of MEMS variable optical attenuator (VOA) devices based on a patented thermal actuator technology. The graphic below shows a cross-section of all layers in the SOIMUMPs process.

1. Starting substrate: N-type double-side polished silicon on insulator (SOI) wafer, consisting of a 10mm Silicon layer, a 1mm Oxide layer, and a 400mm Substrate layer. A Bottom Side Oxide layer that is slightly thinner than the Oxide layer is also present on the bottom side of the Substrate layer.

2. The top surface of the Silicon layer is doped by depositing a phosphosilicate glass (PSG) layer and annealing at 1050°C for 1 hour in Argon. This PSG layer is then removed.

3. The Silicon is lithographically patterned with the first mask level, SOI, and deep reactive ion etched (DRIE) etched. A frontside protection material is then applied to the top surface of the Silicon layer.

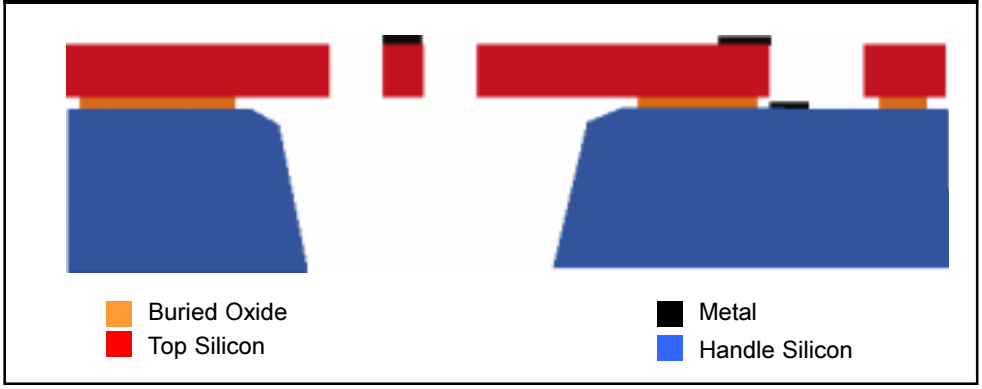
4. The Substrate layer is then lithographically patterned from the bottom side using the second mask level, TRENCH. This pattern is then reactive ion etched (RIE) into the Bottom Side Oxide layer. A DRIE silicon etch is subsequently used to etch these features completely through the Substrate layer

5. Dry processes are used to remove both the protection material and Oxide layer in the regions defined by the TRENCH mask. This step can be used to “release” any mechanical structures in the Silicon layer that are located over through-holes defined in the Substrate layer.

6. The Metal layer, consisting of 50nm Cr + 600nm Au, is deposited and patterned using a shadow masking technique.

7. The wafers are diced using scribe and break method, sorted and shipped to the SOIMUMPs user.

Cross Section of All Layers in SOIMUMPs



is standardized.

The ability to fabricate thick structures that provide better control over key mechanical parameters such as flatness and stiffness has made SOI processing an increasingly popular MEMS fabrication tool. The process is based on a proven process flow that has been used to fabricate high volume commercial optical products. As such, SOIMUMPs provides a robust platform for the development of a number of different MEMS structures, including thermal and electrostatic actuators, and a wide variety of optical telecom devices such as variable optical attenuators (VOA) and one and two degree(s) of freedom rotating mirrors.

All of MEMSCAP’s MUMPs® offerings rely on the internet to facilitate the program. Users may download design rules, view run schedules and pricing, and reserve die space on the MUMPs® website. The schedule is structured to allow users to fabricate on a regular, uninterrupted cycle. Time is allocated between the shipment of one run and the design deadline of the next run, allowing for test and evaluation of fabricated devices in time to redesign for the next scheduled run.

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