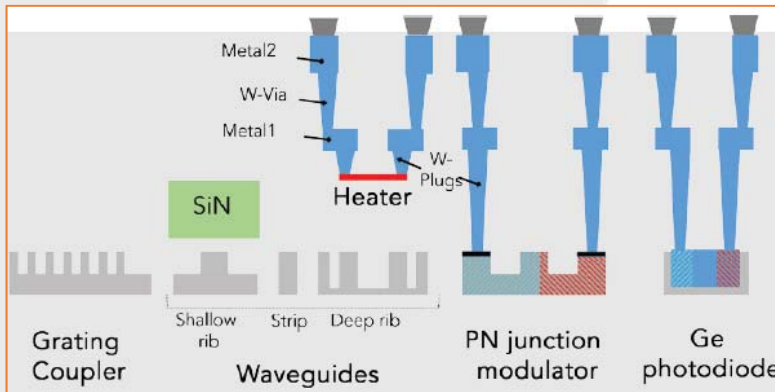


# Silicon Photonic ICs Prototyping & Low Volume Production

Circuits Multi Projets®/ Multi-project circuits® (CMP) provides access to the **Si310-PHMP2M technology** from **CEA-LETI** in the frame of IRT Nanoelec for MPW prototyping and low volume production of Silicon Photonic ICs.

## Si310-PHMP2M Technology



### Advanced structures

- 200mm **SOI substrate** with 310nm Si and 2µm buried oxide
- **Multilevel patterning**
- **Silicied** modulator contacts
- 2 metal layers
- **SiN** layer

### Integration of additional functions

- Passive components
  - \* Shallow, deep rib and strip WG
  - \* **1 & 2D** grating couplers
- Active components
  - \* High speed **Photodetectors**
  - \* High speed **Modulators**

### High performance building blocks

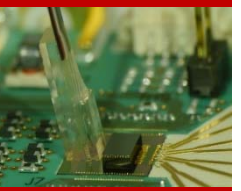
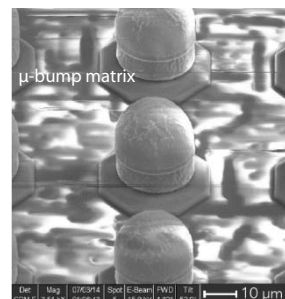
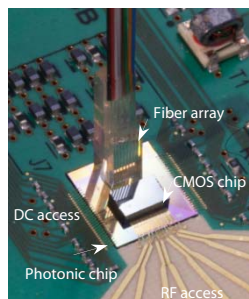
- Fixed cells, Parametrised Cells and Black boxes
- Devices operating at O-Band and C-Band

**PDKs** for Cadence, Mentor Graphics & Synopsys design platforms

### Platform Compatible with Open 3D Post-processes

#### Available options

- Optical edge coupler
- Under Bump Metallization
- Bumps & µ-Bumps deposition



#### Multi-Project Circuits®

CMP is a service organisation in ICs, Photonics & MEMS for prototyping and low volume production. Circuits are fabricated for Universities, Research Laboratories and Industrial companies

#### CAD, design kits and support

CMP distributes design kits for all technologies available through CMP and for the most of the CAD tools. Some specific support is given to CMP customers for MEMS design.

#### Packaging

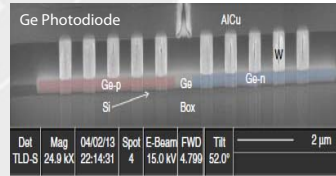
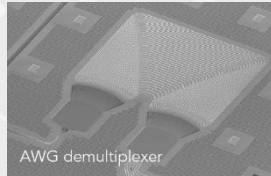
**Standard packaging**  
Ceramic : QFPF, DIL, LCC, JLCC, PGA, SOIC, QFN...  
Plastic : BGA, QFN, QFP, PLCC, SOIC, TSSOP

**MEMS packaging**  
Optical resin/Chip On Board (COB)/Thermal solutions/Metallic package/Hermetic package

**Advanced packaging**  
OPEN 3D post-process, Si interposer, Wafer level bumping, Flip Chip and stacked chip

# Silicon Photonic ICs

## Si310-PHMP2M library contents & indicative performances



### Passive components

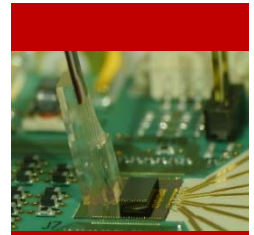
Component	Specifications	Indicative value	
		1310nm	1550nm
Rib waveguide	Loss	<0.4 dB/cm	<1 dB/cm
Strip waveguide	Loss	<2 dB/cm	<5 dB/cm
Deep Rib waveguide	Loss	<3 dB/cm	<4.5 dB/cm
Rib multimode waveguide	Loss	<0.2 dB/cm	<0.2 dB/cm
Transitions	Loss	<0.03 dB	<0.03 dB
Fiber grating coupler 1D	Insertion loss	<2.4 dB	<2.5 dB
	Central wavelength	1310 nm	1550 nm
	1dB bandwidth	27 nm	30 nm
Fiber grating coupler 2D	Insertion loss	<5 dB	<3.5 dB
	Peak wavelength	1310 nm	1550 nm
	1dB bandwidth	25 nm	25 nm
Directional coupler	Loss	<0.05 dB	<0.06 dB
Ring filter	Loss	< 0.5 dB	< 0.5 dB
	Extinction ratio	>15 dB	>15 dB
	Quality Factor	>10,000	>10,000
MMI 1x2	Loss	<0.1 dB	<0.2 dB
	Output balance	+/- 1%	+/- 2%

### Active components

Component	Specifications	Indicative value	
		1310nm	1550nm
Mach Zehnder modulator (3mm long)	OE bandwidth @-4V	40 GHz	40 GHz
	Loss junction	< 1 dB/mm	< 0.8 dB/mm
	VpiLpi @-2V	< 1.5 V.cm	< 2 V.cm
Ring Racetrack modulator	OE bandwidth @-2V	>15 GHz	>15 GHz
	Insertion loss	<0.5 dB	<0.5 dB
	VpiLpi @-2V	<2.5 V.cm	<2.5 V.cm
Ge Photodiode PiN longitudinal	EO bandwidth @-1V	>35 GHz	>35 GHz
	Responsivity @-1V	>0.75 A/W	>0.7 A/W
	Dark current @-1V	<50 nA	<55 nA

Contacts : François Berthollet  
[Francois.Berthollet@mycmp.fr](mailto:Francois.Berthollet@mycmp.fr)  
 +33 476 574 621

André Myko  
[Andre.Myko@cea.fr](mailto:Andre.Myko@cea.fr)  
 +33 438 784 164



### Multi-Project Circuits®

CMP is a service organisation in ICs, Photonics & MEMS for prototyping and low volume production. Circuits are fabricated for Universities, Research Laboratories and Industrial companies

### CAD, design kits and support

CMP distributes design kits for all technologies available through CMP and for the most of the CAD tools. Some specific support is given to CMP customers for MEMS design.

### Packaging

*Standard packaging*  
 Ceramic : CQPF, DIL, LCC, JLCC, PGA, SOIC, QFN...  
 Plastic : BGA, QFN, QFP, PLCC, SOIC, TSSOP

*MEMS packaging*  
 Optical resin/Chip On Board (COB)/Thermal solutions/Metallic package/Hermetic package

*Advanced packaging*  
 OPEN 3D post-process, Si interposer, Wafer level bumping, Flip Chip and stacked chip