



IRT Nanoelec and CMP Announce World's First Multi-Project Wafer Service with Silicon Photonics on 310nm SOI Platform

GRENOBLE, France – 11 July, 2016 – IRT Nanoelec, an R&D consortium focused on information and communication technologies (ICT) using micro and nanoelectronics, and CMP, Circuits Multi-Projets®, a service organization in ICs and MEMS prototyping and low volume production, today announced the IC industry's first multi-project wafer (MPW) process for fabricating silicon-photonics devices on a 310nm silicon on insulator (SOI) platform. The MPW service also includes compatible IC MPW services and the first service for post-process 3D integration on multi-project wafers. IRT, which is headed by CEA-Leti, and CMP announced that service in 2015.

Available on Leti's 200mm CMOS line, the MPW service provides a comprehensive, very low-cost way to address the challenges of achieving miniaturization and high-density components. An electronic chip can be flip chip assembled on top of the photonics chip.

"Fabricating photonics technology on silicon is complex and costly, which has been an entry barrier for many research organizations and fabless companies," said Maryse Fournier, IRT MPW Project Manager. "This MPW capability on a 310nm SOI platform provides drastic cost-saving advantages, and opens the door for them to create products for long-haul telecom, short-reach datacom, optical switching in datacenters and other markets that require the speed and capacity that silicon photonics offers." This technology offer comes with a Design Kit, including layout, verification and simulation capabilities. Libraries are provided with comprehensive list of active and passive electro-optical components. The design kit environment is compatible with full 3D integration offers through CMP.

"This Silicon Photonics 310nm on SOI, multi-project wafer capability along with complementary 3D post-process services bring our IC community another step closer to a complete process, which includes through-silicon-via last, fine-pitch vertical interconnects and specific finishing for 3D integration like under-bump metallization," said Jean-Christophe Crébier, Director of CMP. "It also can significantly speed the development of new silicon-photonics devices that meet constantly growing data-handling requirements."

About IRT-Nanoelec Research Technological Institute (IRT)

Nanoelec Research Technological Institute (IRT), headed by CEA-Leti conducts research and development in the field of information and communication technologies (ICT) and, specifically, micro- and nanoelectronics. Based in Grenoble, France, IRT Nanoelec leverages the area's proven innovation ecosystem to create the technologies that will power the nanoelectronics of tomorrow, drive new product development and inspire new applications – like the Internet of Things – for existing technologies. The R&D conducted at IRT Nanoelec provides early insight into how emerging technologies such as 3D integration and silicon photonics will affect integrated circuits. Visit www.irtnanoelec.fr.

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About CMP

CMP is a service organization in ICs and MEMS for prototyping and low volume production. CMP enables prototypes fabrication on industrial processes at very attractive costs and offers it great technical expertise in providing MPW and related services for Universities, Research Laboratories and Industrial companies' prototyping. Chips are normally untested and delivered packaged or not. Advanced industrial technologies are made available in CMOS, SiGe BiCMOS, HV-CMOS, SOI, MEMS, 3D-IC, etc. Since 1981 more than 1000 Institutions from 70 countries have been served, more than 7000 projects have been prototyped through a thousand runs, and 71 different technologies have been interfaced. For more information, visit: <http://cmp.imag.fr>

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