ORDER FORM FOR ICs MANUFACTURING

For laboratories which are STMicroelectronics partners

CMP RUN: TOPCELL NAME[1]: PROCESS:

DELIVERY & INVOICING

CIRCUIT'S PURPOSE: ☐ Education ☐ Research ☐ Industry

INSTITUTION/COMPANY:

DELIVERY TO: Name: Phone:
Institution/company:
Full address (no PO box):

SPECIAL REQUEST ON DELIVERY: ☐ yes ☐ no
If no, circuits will be sent by courier service (UPS, DHL…) with our standard 'invoice for customs' for foreign countries.

INVOICE TO: Name: **Andreia Cathelin** Email: Andreia.Cathelin@st.com
Institution/Company: STMicroelectronics
Address: 850 rue Jean Monnet
38926 CROLLES CEDEX
FRANCE

CIRCUIT SIZE IN MICRONS: DeltaX = µm
DeltaY = µm

NUMBER OF PARTS[2] Bare dies: Packaged:

PACKAGE:

Pad type: ☐ wire bond ☐ test probe ☐ flip chip

Bonding diagram[3]: ☐ free ☐ imposed

lids: ☐ removable ☐ sealed

COLOR PLOTS: ☐ yes ☐ no number:

NON-STANDARD DIE THICKNESS[4]**: µm**

ADDITIONAL SERVICES[5]:

Reserved to CMP& ST
area:
Cost Center:
IFRS:
Set-up:
price:
NRE:
price:
price:
price:
shipment:
Total:

By signing the present order form, the responsible person accepts the Terms and Conditions that are in https://mycmp.fr/services/terms-and-conditions.html
Name and signature of the responsible person:

Name: date: signature:

Signature of Andreia Cathelin date: signature:

ORDER FORM FOR ICs MANUFACTURING

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CMP RUN: TOPCELL NAME[1]: PROCESS:

TECHNICAL INFORMATION

TECHNICAL ENQUIRIES[6]: Name: Phone:
E-mail:

CIRCUIT TRANSFER: ☐ web account (default) ☐ ftp (files > 20MB)
DESCRIPTION FORMAT[7]: ☐ GDSII Other:

CAD TOOL: version:
DESIGN KIT: version:
DRC VIOLATIONS: ☐ yes ☐ no *If you request DRC violations, please make a case overleaf.*

LIBRARY CELL REPLACEMENT REQUIRED[8]: ☐ yes ☐ no
(make a list of used libraries)
LIBRARY NAME version

ST Project Plan[9] (Mandatory)**:**

CIRCUIT FUNCTION *(Mandatory, a few lines in English):*

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DON'T SEND THIS PAGE

This order form is reserved to circuits that are sent as part of a cooperation between STMicroelectronics and Laboratories.

Send it signed by Email to Andreia Cathelin with a copy to CMP.

Only delivery of 25 bare dies is payed out by STMicroelectronics. Additional services like color plots, packaging and additional dies are charged to the designer.

RESERVATION REQUEST

You must send a CMP Order Form and a reservation request ***at least one month before the deadline*** of the run. Please contact us for document for reservation request.

PACKAGES

Packaging service is available if you are following packaging rules of CMP. Prices, list of packages and cavity maps are in:
https://mycmp.fr/ -> Technologies -> Packaging
https://mycmp.fr/ -> Technologies -> Price list -> CMP price list (right column)

Contact us for unlisted ceramic packages, we will check with our subcontractors.

Contact us for plastic packages. Small sets of plastic packages are possible. Main packages are SOIC, SSOP, LPCC (leadless), QFP, PLCC and EDQUAD (thermal solution).

NB: Design your pad ring according to the chosen package. Long wires and big angles are accepted for prototypes in ceramic packages and in open cavity packages but they are decreasing circuit performances. Packaging rules for plastic are strict for wire length and for angles of wires.

NOTES

(1) Maximum 8 characters (letters, digits and "_") for ST database, the first character must be a letter.

(2) Default is 25 bare dies for our main technologies. Additional dies, color plots and packaging are charged.

(3) Free means that CMP will make a bonding diagram and send it to you for approval. Note that CMP can't make bonding diagrams if the pad ring doesn't match with cavity of the selected package. If you send your bonding diagram please clearly identify pad #1 in your circuit.

(4) Standard die thicknesses (T) are as following. You can request another thickness for your application. Contact us for cost and delay. "T*" means that die thickness can't be changed. Minimum thickness is 120µm for circuits smaller or equal to 3mm x 3mm.
STMicroelectronics: 130nm: T= 375µ 65nm: T=250µ 55nm: T= 250µ 28nm: T=250µ BCD8SP: T= 280µ

(5) If you need any other service, contact us to check if we can provide it.

(6) The person given on the form under the heading "TECHNICAL ENQUIRIES" must be rapidly available for questions and corrections of the design. The designer is generally the best choice.

(7) For other format than gds2 contact CMP for an authorization.

(8) Layout descriptions of library cells of STMicroelectronics contain only metal layers. For these technologies, library cells have to be replaced by the full layout version. **You must request replacement** and provide CMP with the list of used libraries and their versions.
NB: names of standard cells are reserved names. Using them for naming custom cell is forbidden otherwise custom cell will be overwritten by standard cell.
Example of request of "LIBRARY CELL REPLACEMENT" for a circuit in HCMOS9GP technology of STMicroelectronics:

IOLIB_65_M6_LL	version 7.1
COR9GPLL	version 4.1
DPHS9gp_1024x32m16d4_L	version DPHS_100327_1

(9) Name of the project at ST or name of the contact person for your circuit at ST.