ORDER FORM FOR ICs MANUFACTURING

CMP RUN: TOPCELL NAME[1]: PROCESS:

DELIVERY & INVOICING

CIRCUIT'S PURPOSE: ☐ Education ☐ Research ☐ Industry

INSTITUTION/COMPANY:
DELIVERY TO: Name: Phone:
Institution/company:
Full address (no PO box):

SPECIAL REQUEST ON DELIVERY: ☐ yes ☐ no
If no, circuits will be sent by courier service (UPS) with our standard 'invoice for customs' for foreign countries.

INVOICE TO: Name: Phone:
E-mail:
Institution/Company: VAT id:
Address: (Europe only)
P.O. number:

CIRCUIT SIZE: DeltaX (µm) =
DeltaY (µm) =

NUMBER OF PARTS[2] Bare dies: Packaged:

PACKAGE:

Pad types: ☐ wire bond ☐ test probe ☐ flip chip[3]

☐ no bump ☐ copper pillars ☐ solder bumps ☐ gold stud bumps

Bonding diagram[4]: ☐ free ☐ imposed

lids: ☐ removable ☐ sealed

BULK MICROMACHINING[5] ☐ yes ☐ no

COLOUR PLOTS: ☐ yes ☐ no number:

NON-STANDARD DIE THICKNESS[6]**:** **µ**

ADDITIONAL SERVICES[7]:

Reserved to CMP
area:
price:
price:
set_up:
NRE:
price:
price:
price:
price:
shipment:
Total:

By signing the present order form, the responsible person accepts the Terms and Conditions that are in https://mycmp.fr/services/terms-and-conditions.html
Name and signature of the responsible person:

Name: date: signature:

ORDER FORM FOR ICs MANUFACTURING

CMP RUN: TOPCELL NAME: PROCESS:

TECHNICAL INFORMATION

TECHNICAL ENQUIRIES[8]: Name: Phone:

E-mail:

CIRCUIT TRANSFER: ☐ web account (default) ☐ ftp (files > 20MB)

DESCRIPTION FORMAT[9]: ☐ GDSII Other:

CAD TOOL: version:

DESIGN KIT: version:

DRC VIOLATIONS: ☐ yes ☐ no *If you request DRC violations, please make a case overleaf.*

LIBRARY CELL REPLACEMENT REQUIRED[10]: ☐ yes ☐ no

(make a list of used libraries)

LIBRARY NAME version

LOW VOLUME PRODUCTION EXPECTED? ☐ yes ☐ perhaps ☐ no

VERSION OF DESIGN THAT SHOULD BE PRODUCED: ☐ this one after test ☐ an improved one

START PRODUCTION: ☐ in next 6 months ☐ < 1 year ☐ > 1 year

EXPECTED NUMBER OF CIRCUITS: ☐ < 100 ☐ < 1000 ☐ < 10000 ☐ > 10000

CIRCUIT FUNCTION *(a few lines in English. Mandatory for non E.U. countries, used for export regulation. Mandatory for technologies of STMicroelectronics. Will be published in the CMP annual repport)*

ORDER FORM FOR ICs MANUFACTURING

DON'T SEND THIS PAGE

RESERVATION REQUESTS

For technologies of STmicroelectronics you must send a reservation request ***one month before the deadline***. Please contact us by Email for the document.

PACKAGING

Packaging service is available if you are following packaging rules of CMP. Prices, list of packages and cavity maps are in:
https://mycmp.fr -> Technologies -> Packaging
https://mycmp.fr -> Technologies -> Price list -> CMP price list (right column)
Contact us for unlisted ceramic packages, we will check with our subcontractors.

Contact us for plastic packages. Small sets of plastic packages are possible. Main packages are SOIC, SSOP, LPCC (leadless), QFP, PLCC and EDQUAD (thermal solution).

NB: Design your pad ring according to the chosen package. Long wires and big angles are accepted for prototypes in ceramic packages and in open cavity packages but they are decreasing circuit performances. Packaging rules for plastic are strict for wire length and for angles of wires.

FLIP-CHIP PACKAGING

For flip-chip assembly please check Check our process catalog:
https://mycmp.fr -> Technologies -> Process catalog
Flip-Chip Packaging (solder bumps, gold stud bumps)
Wafer-level packaging (copper pillars)
WARNING: There is no standard package for flip-chip packaging. You have to create your dedicated package.

NOTES

(1) Maximum14 characters, the first character must be a letter.

(2) Default is 25 bare dies for our main technologies. Additional dies, color plots and packaging are charged.

(3) If you request generation of bumps by CMP your flip chip pads have to match with CMP's design rules. Rules depend on the type of bumps. If bumps are generated by your subcontractor, select "no bump" next line.
Note that bumps are not generated by CMP in all CMP runs.

(4) Free means that CMP will make a bonding diagram and send it to you for approval. Note that CMP can't make bonding diagrams if the pad ring doesn't match with cavity of the selected package. If you send your bonding diagram please clearly identify pad #1 in your circuit.

(5) Micromechanical systems are available only on ams 0.35µ technologies.

(6) Standard die thicknesses (T) are as following. You can request another thickness for your application. Contact us for cost and delay. "T*" means that die thickness can't be changed. Minimum thickness is 120µm for circuits smaller or equal to 3mm x 3mm.

ams:	0.35µ: T= 530µ	0.18µ: T= 530µ				
STMicroelectronics:	130nm: T= 375µ	65nm: T=250µ	55nm: T= 250µ	28nm: T=250µ	BCD8SP: T= 280µ	

(7) If you need any other service, contact us to check if we can provide it.

(8) The person given on the form under the heading "TECHNICAL ENQUIRIES" must be rapidly available for questions and corrections of the design. The designer is generally the best choice.

(9) For other format than gds2 contact CMP for an authorization.

(10) Layout descriptions of library cells of STMicroelectronics contain only metal layers. For these technologies, library cells have to be replaced by the full layout version. **You must request replacement** and provide CMP with the list of used libraries and their versions.
NB: names of standard cells are reserved names. Using them for naming custom cell is forbidden otherwise custom cell will be overwritten by standard cell.
Example of request of "LIBRARY CELL REPLACEMENT" for a circuit in CMOS28FDSOI technology of STMicroelectronics:

C28SOI_IO_EXT_ANAF_ANA_EG	version 7.0
C28SOI_SC_12_CORE_LL	version 5.1
ST_SPHD_HIPERF_8192x32m32_bTlmr	version SPHD_HIPERF_180128