From layout to chips

CMP is about to provide access to

NEW

em microelectronic

DK access from Q3 2019

Technology offering overview

	Minimum Gate Length:	Dual Gate Oxides:	# Metal Layers	FEOL Isolation
0.18µm **EMALPC18** logic	180nm [drawn]	3.0nm ThinGOX [1.98V max] 6.5nm DualGOX [3.63V max]	4/5 Metal Layers: AlCu: option B -4 ML or option M -5 ML	Non Epi or p-Epi substrate [16-24Ω.cm] STI [Shallow trench Isolation]

Analog Low Power

- Ultra-Low power
- Low Vth
- Low leakage

Sept-19

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European Commission

EUROPRACTICE IC SERVICE

Price / Schedule / General information

NEW

From layout to chips

MPW SCHEDULE 2020*	A	M	J	J	A	S	O	N	D	Standard price in Euro/mm²	Discount in Euro/project**
EMALPC18 technology	24			31			30			**1950 Euro/mm² for Area < 5mm²** **1250 Euro/mm² for mm² above 5mm²**	**600**

Price = area (mm²) X price/mm² with minimum fabrication cost equivalent to 2,35 mm²
*** MPW scheduled runs are subject to modification**
**** For active Europractice IC member only.**

TECHNOLOGY CHARACTERISTICS:

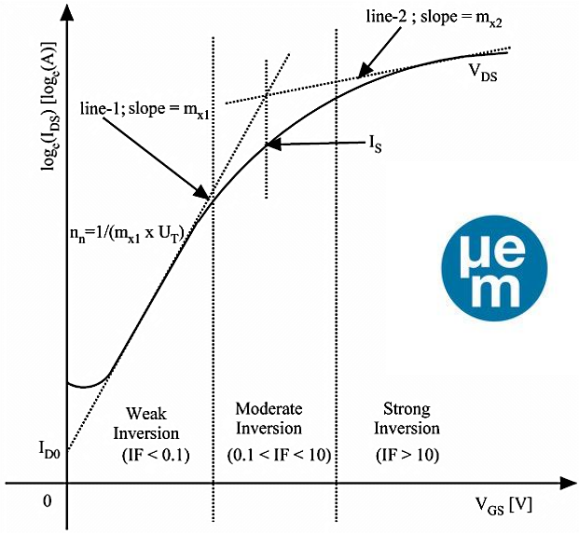
Key features: 8 inch Fab, fully manufactured in Switzerland

- 180 nm – Including accurate devices, **optimized for Analog**
- Developed for **Ultra Low Power, Ultra Low Voltage** Designs
- **EKV accurate** model/parameters for **near threshold** bias

Ultra low power, horlogy, sensors, IoT, Mixed analog/digital

Advanced models for accurate simulations, Standard logic & IO cells, advanced devices & IPs,.

Dedicated runs available on request.



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