FD-SOI Design Techniques Tutorial Day

In the frame of the SOI Consortium Symposium

San Jose, April 14th, 2017

Organizer: Andreia Cathelin, STMicroelectronics

Mentors: Carlos Mazuré and Giorgio Cesana, SOI Industry Consortium

8.00 – 8.30: breakfast

8.30- 9.30: Andreia Cathelin, Fellow, STMicroelectronics Crolles, France

FDSOI short overview and advantages for analog, RF and mmW design

Abstract: This talk will first present a very short overview of the major analog and RF technology features of 28nm FDSOI technology. Then we will focus on the benefits of FD-SOI technology for analog/RF and millimeter-wave circuits, by taking full advantage of wide voltage range body biasing tuning. For each category of circuits (analog/RF and mmW), concrete design examples such as analog low-pass filter and 60GHz Power Amplifier are given in order to highlight the main design features specific to FD-SOI and the resulting performances.

9.30 – 10.30: Sorin Voinigescu, Professor, University of Toronto, Toronto, Canada

Unique circuit topologies and back-gate biasing scheme for RF, mm-wave and broadband circuit design in FDSOI technologies

Abstract: This presentation will discuss the main features of FD-SOI CMOS technology and how to efficiently use them in RF, mm-wave and broadband fiber-optic SoCs. First, a transistor level overview will be given, presenting the impact of the back-gate bias on the measured I-V, transconductance, fT and fMAX characteristics and comparing the MAG of FDSOI MOSFETs with those of planar bulk CMOS and SiGe BiCMOS transistors through measurements up to 325 GHz. Next, the presentation will provide design examples of LNA, mixer, switches, CML logic and PA circuit topologies and layouts that make efficient use of the back-gate bias to overcome the limitations associated with the low breakdown voltage of sub-28nm CMOS technologies. Finally, a 60Gb/s large swing driver in 28nm FDSOI CMOS for a large extinction-ratio 44Gb/s SiPh MZM 3D-integrated module will be described, as a practical demonstration of the unique capabilities of FDSOI technologies which cannot be realized in FiNFET or planar bulk CMOS.

10.30 – 11.00: break

11.00 – 12.00: Joachim Rodrigues, Professor, Lund University, Lund, Sweden

Design strategies for ULV memories in 28nm FDS-SOI

Abstract: In this tutorial two different design strategies for ultra-low voltage (ULV) memories in 28nm FD-SOI are presented. For small storage capacities, e.g., below 4kb, the design of standard-cell based memories (SCM), which is based on a custom latch, is discussed. Trade-offs for area cost, leakage power, access time, and access energy are discussed and realized using different read logic styles. It will be shown how the full custom latch is seamlessly integrated in an RTL-GDSII design flow. Furthermore, the characteristics of a 28nm FD-SOI 128 kb ULV SRAM, based on a 7T bitcell with a single bitline, will be disclosed. It will be shown how the overall energy efficiency is enhanced by optimizations on all abstraction levels, i.e., from bitcell to macro integration. Degraded performance and reliability due to ULV operation is recovered by selectively overdriving the bitline and wordline with a new single-cycle charge-pump. A dedicated sense-amplifierless read architecture with a new address-decoding scheme delivers 90MHz read speed at 300mV, dissipating 8.4 fJ/bit-access. All performance claims are based on silicon measurements.

12.00 – 13.00: lunch

13.00 – 14.00: Bora Nikolic, Professor, UC Berkeley, Berkeley, USA

Energy-Efficient Processors in 28nm FDSOI

Abstract: This talk presents the design of a series of energy-efficient microprocessors. They are based on an open and free Berkeley RISC-V architecture and implement several techniques for operation in a very wide voltage range utilizing 28nm FDSOI. To enable agile dynamic voltage and frequency scaling, with high energy efficiency the designs feature an integrated switched-capacitor DC-DC converter. A custom-designed SRAM-based cache operates in a wide 0.45-1V supply range. Techniques that enable low-voltage SRAM operation include 8T cells, assist techniques and differential read. Techniques specific to FDSOI design will be discussed in detail.

14.00 – 15.00: Boris Murmann, Professor, Stanford University, Palo Alto, USA

Pushing the envelope in mixed-signal design using FD-SOI

Abstract: FD-SOI technology blends high integration density with outstanding analog device performance. In this presentation, we will review the specific advantages that FD-SOI brings to the design of mixed-signal blocks such as data converters and switched-capacitor blocks. Following the review of such general benchmarking data, we will show concrete design examples including an ultrasound interface circuit, a mixed-signal compute block, and a mixer-first RF front-end.

About the instructors:

Andreia Cathelin started electrical engineering studies at the Polytechnic Institute of Bucarest, Romania and graduated from the Institut Supérieur d'Electronique du Nord (ISEN), Lille, France in 1994. In 1998 and 2013 respectively, she received PhD and "habilitation à diriger des recherches" (French highest academic degree) from the Université de Lille 1, France.

In 1997, she was with Info Technologies, Gradignan, France, working on analog and RF communications design. Since 1998, she has been with STMicroelectronics, Crolles, France, and now Fellow in the Technology R&D Group. Her major fields of interest are in the area of RF/mmW/THz systems for communications and imaging. She is leading and driving research in such advanced topics by supervising company internal PhD's and through cooperation with major universities around the world. She has also management activities as being in charge of the ST-CMP operation (the CMP is an independent organization offering small series foundry services for SME and research institutes). Finally she actively supports the promotion of all advanced technologies developed in the company. Andreia is serving in several IEEE conferences and committees. She has been active at ISSCC as RF sub-committee chair from 2012 to 2015, and is currently Forums Chair and member of the Executive Committee. She is member of ESSCIRC TPC since 2005 and is currently the ESSCIRC-ESSDERC Steering Committee Chair. She has been on the Technical Program Committees of VLSI Symposium on Circuits from 2010 till 2016, serving in the last years as officer. She has been Guest Editor of the IEEE JSSC Special Issue on VLSI Symposium in April 2016. Andreia has authored or co-authored 100+ technical papers and 4 book chapters, and has filed more than 25 patents. Andreia is a co-recipient of the ISSCC 2012 Jan Van Vessem Award for Outstanding European Paper and of the ISSCC 2013 Jack Kilby Award for Outstanding Student Paper; as well as winner of the 2012 STMicroelectronics Technology Council Innovation Prize. The 60GHz transceiver resulting of a joint research between STMicroelectronics and CEA-Leti to which Andreia has actively participated has been selected as cover photo for the International Seventh Edition (Oxford University Press 2016) of the famous Adel S. Sedra and Kenneth C. Smith Microelectronics Circuits book. She is an elected member of the IEEE SSCS Adcom for the term January 2015 to December 2017.

Sorin P. Voinigescu graduated in 1984 with a M.Sc. degree in Electronics from the Polytechnic Institute of Bucharest, Romania. He received the Ph.D. degree in Electrical and Computer Engineering from the University of Toronto, Canada, in 1994. His Ph.D. dissertation was on the design and fabrication of VLSI compatible Si/SiGe p-MOSFET's. Between 1984 and 1991 he worked in R&D and in academia in Bucharest, designing and lecturing on microwave semiconductor devices and microwave integrated circuits. Between 1994 and 2000 he was with NORTEL NETWORKS in Ottawa where he was responsible for projects in high-frequency characterization and statistical scalable compact model development for Si, SiGe and III-V heterostructure devices. He spearheaded the modeling infrastructure development for, and was involved in the prototyping of wireless and broadband fiber optics transceivers in emerging semiconductor technologies. In April 2000 he co-founded Quake Technologies Inc. an Ottawa-area fabless semiconductor company focussing on the design and

fabrication of 10 Gb/s and 40 Gb/s Physical Layer ICs. Quake was acquired by AMCC in 2006. As Chief Technology Officer at Quake he coordinated the access and characterization of Si, SiGe, GaAs and InP technologies, high-frequency package design and electro-optical interface integrated circuits development. In September 2002 he joined the Electrical and Computer Engineering Department at the University of Toronto where he is a full Professor. His research and teaching interests focus on the modelling, characterization and fabrication of nanoscale and atomic-scale electronic devices and technologies, and on design techniques and circuit topologies for mm-wave DSP, radio, radar and imaging ICs operating in the 50 to 500-GHz range. Dr Voinigescu is an IEEE Fellow.

Joachim Neves Rodrigues holds currently an associate professorship at the digital circuit design group at the department of Electrical and Information Technology. He is currently the Chair of the Swedish SSC chapter, and since 2017 he is the Vice-Director of Industrial Excellence Center in System Design on Silicon. From 2012-16 he served as the Program Director for Embedded Electronics Engineering (former System-on-Chip). Furthermore, between 2008 and 2016 he was active as external associate professor at the Department of Informatics and Mathematical Modelling at Denmark Technical University. After receiving his PhD degree from Lund University in circuit design in 2005 he joined the multimedia ASIC group at Ericsson Mobile Platforms (EMP), Lund, Sweden. At EMP (now Ericsson) he held the position as digital ASIC process lead. Joachim obtained his degree in Electronic Engineering and Computer Science at the Hochschule Kaiserslautern, Germany, in 1999. His research interest is energy efficient ASIC implementation of algorithms in the biomedical area. In 2008 Joachim was awarded with the LTH postdoc grant for young researchers. In 2011 he received a research grant for young researchers from Vetenskapsrådet for "Design strategies for digital ultra-low energy circuits", followed by a second grant in 2017 for “Ultra Low Voltage SRAM Architectures- Assist circuitry and Logic in Memory”.

Borivoje Nikolić is the National Semiconductor Distinguished Professor of Engineering at the University of California, Berkeley. He received the Dipl.Ing. and M.Sc. degrees in electrical engineering from the University of Belgrade, Serbia, in 1992 and 1994, respectively, and the Ph.D. degree from the University of California at Davis in 1999.

His research activities include digital, analog and RF integrated circuit design and communications and signal processing systems. He is co-author of the book Digital Integrated Circuits: A Design Perspective, 2nd ed, Prentice-Hall, 2003. Dr. Nikolić received many awards in his career, including the NSF CAREER award in 2003, and the best paper awards at the IEEE International Solid- State Circuits Conference, Symposium on VLSI Circuits, IEEE International SOI Conference, European Solid-State Circuits Research Conference, European Solid-State Device Research Conference, S3S conference and the ACM/IEEE International Symposium of Low- Power Electronics. Dr Nikolic is an IEEE Fellow.

Boris Murmann joined Stanford University in 2004 and currently serves as a Professor of Electrical Engineering. He received the Ph.D. degree in electrical engineering from the University of California at Berkeley in 2003. From 1994 to 1997, he was with Neutron Microelectronics, Germany, where he developed low-power and smart-power ASICs in automotive CMOS technology. Dr. Murmann's research interests are in the area of mixed-signal integrated circuit design, with special emphasis on data converters and sensor interfaces. In 2008, he was a co-recipient of the Best Student Paper Award at the VLSI Circuits Symposium and a recipient of the Best Invited Paper Award at the IEEE Custom Integrated Circuits Conference (CICC). He received the Agilent Early Career Professor Award in 2009 and the Friedrich Wilhelm Bessel Research Award in 2012. He has served as an Associate Editor of the IEEE Journal of Solid-State Circuits and as the Data Converter Subcommittee Chair of the IEEE International Solid-State Circuits Conference (ISSCC). He is the program chair for the ISSCC 2017 and a Fellow of the IEEE.