ICs, Si-Photonics, 3D-ICs & MEMS, Smart Power, Prototyping & Low Volume Production

Circuits Multi-Projets® (CMP) is a Multi-Project Wafer (MPW) service organization providing support for cost effective prototyping and low volume production. Circuits are fabricated on matured process lines for academics and industrial.

Since 1981, 619 customers from 70 countries have been served, more than 8100 projects have been prototyped through 1103 MPW runs and 73 different technologies have been interfaced.

CMP distributes Design-Kits (DK) for all of them. They contains technology files, simulation models, design rules, standard cell libraries. Requested design kit can be sent to customer after a non-disclosure agreement (NDA) with CMP.

Design-Kit Request Form->https://mycmp.fr/requests/design-kit-dk Contact: Sylvaine EYRAUD->[Sylvaine.Eyraud@mycmp.fr]  
Design-Kit Support Center->https://mycmp.fr/requests/support Contact: Christelle RABACHE->[Christelle.Rabache@mycmp.fr]

CMOS/BiCMOS/SiGe Integrated Circuits

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Non-Volatile Memory (NVM) Integrated Circuits

IRT Nanoelec/LETI-CEA  OxRAM NVM on 130nm CMOS  MAD200

Silicon Photonic Integrated Circuits

IRT Nanoelec/LETI-CEA  Silicon PIC  Si310–PHMP2M

MEMS - Micro Electro Mechanical Systems

ams 0.35μm  CMOS Bulk Micromachining: Front-side & Back-side Micromachining
MEMSCAP  PolyMUMPs - SOIMUMPS- PiezoMUMPs
Teledyne DALSA  MIDIS™

Discounts & discount prices, when applicable, are applied to most MPW services. Prices on the Web site.
CMP offers a wide variety of standard packages and assembly services for prototyping and low volume production. Before starting a design, an important step is to select a package and packaging technic. Die package compatibility optimization can significantly impact the overall system performances.

**Standard packaging**

Complete assembly service based on a wide range of ceramic and plastic packages for prototyping and low volume production. Die pad ring has to match with package cavity.

**Ceramic:** CQFP, DIL, LCC, LCCC, PGA, SOIC, QFN...

**Plastic:** BGA, QFN, QFP, PLCC, SOIC, TSSOP...

**Advanced packaging**

Designers are supported every step of the way, from the installation and use of the PDK 3D Add-on to the final assembly-level verifications of your 3D project, which requires a specific and individual follow-up.

**OPEN 3D post-processes** in partnership with CEA/LETI in the frame of IRT Nanoelec

Set of post-processes allowing 3D interconnection integration at wafer-level, on various technology nodes after standard MPW & dedicated runs opened on STMicroelectronics CMOS065, CMOS028FDSOI, BiCMOS055, BiCMOS9MW and ams C35B4M3. MPW run opened once a year (check on the Web site).

- **Front-side modules:** µ-Bumps / UBM
- **Back-side modules:** TSV last + RDL + Bumps

Various types of assemblies supported:
- Single Die bumping for **Flip-Chip packaging**
- **Die-to-die** stacking
- 2.5D integration on **Silicon interposer**.

40 pieces delivered, prices available on the Website.

**Silicon Interposer MPW runs** in partnership with ams

2.5D Si-Interposer design and prototyping, support for dedicated assembly as an option.
- Both **active** (Frontend + Backend) and **passive** (Backend only) MPW runs are available
- Based on ams C35 4 layers metal stack (3 + 1 Thick)
- UBM deposited at wafer level (Ni/Pd/Au).

40 pieces delivered, prices available on the Website.

**Wafer-level bumping post-process by ST microelectronics**

Features:
- Available on ST 300mm (on CMOS28FDSOI / BiCMOS55 / CMOS065) processes
- UBM process
- Pillar of copper & alloy capping
- Small Diameter & fine pitch

**Hybrid packaging MEMS /Si Photonic + CMOS**

Optical resin, Chip On Board (COB), Thermal solutions, Metallic package, Hermetic sealing.

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*Prices on the Website.*