ICs, Photonics, & MEMS Prototyping & Low Volume Production

46, Avenue Félix Viallet
38000 Grenoble, France
Ph. : +33 4 76 57 46 17
Fax: +33 4 76 47 38 14
cmp@mycmp.fr
mycmp.fr

Circuits Multi-Projets® (CMP) is a Multi-Project Wafer (**MPW**) service organization in Integrated Circuits (ICs), Photonic ICs and Micro Electro Mechanical Systems (MEMS) for **prototyping and low volume production**. Circuits are fabricated using **industrial process lines for universities, research laboratories and industrial companies**. Since 1981, 614 customers from 70 countries have been served, more than 7900 projects have been prototyped through 1043 MPW runs and 72 different technologies have been interfaced.

CMP distributes Process Design-Kits (**PDK**) for CMOS/BiCMOS IC's, Photonic IC's and MEMS' technologies . Each of them contains technology files, simulation models, design rules, standard cell libraries. A copy of any requested design kit can be sent to customer after a non-disclosure agreement (NDA) with CMP. Customer request and support are provided through our Web interfaces:

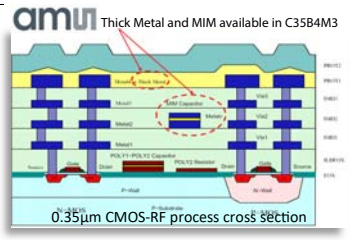
Design-Kit Request Form-> http://mycmp.fr/requests/design-kit-dk
Design-Kit Support Center: http://mycmp.fr/requests/support

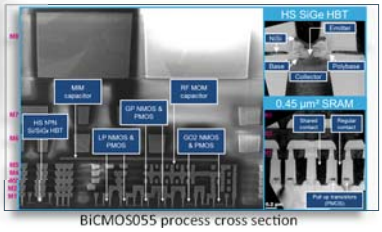
Contact us

Request Form: Sylvaine EYRAUD [Sylvaine.Eyraud@mycmp.fr]
Support Center: Christelle RABACHE [Christelle.Rabache@mycmp.fr]

CMOS/BiCMOS/SiGe Integrated Circuits

ams 0.18µm	***CMOS***	C18A6
	HV-CMOS	H18A6
	BUMPING	on individual project
ams 0.35µm	***CMOS***	C35B4C3
	CMOS-RF	C35B4M3
	SiGe BiCMOS	S35D4M5
	CMOS-Opto BARC	C35B40A
	CMOS-Opto ARC	C35B401
	HV-CMOS	H35B4D3
	BUMPING	on individual project
ST 28nm	***FDSOI***	CMOS28FDSOI
ST 55nm	***SiGe***	BiCMOS055
ST 65nm	***CMOS***	CMOS065
ST 130nm	***SiGe***	BiCMOS9MW
	CMOS	HCMOS9GP
	HV-CMOS	HCMOS9A
	SOI	H9SOI-FEM
new **ST 0.16µm**	***BCD***	BCD8sP
	BCD-SOI	BCD8s-SOI

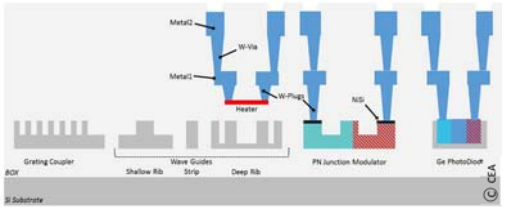




Silicon Photonic Integrated Circuits

IRT Nanoelec/LETI-CEA

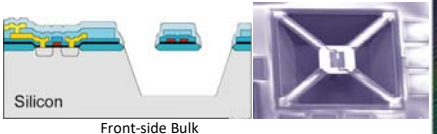
Si310–PHMP2M



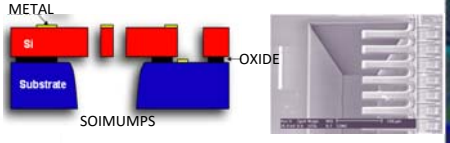
Si310–PHMP2M process

MEMS - Micro Electro Mechanical Systems

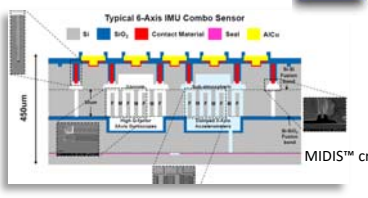
ams 0.35µm	***CMOS Bulk Micromachining: front-side & back-side***
MEMSCAP	***PolyMUMPs***
	SOIMUMPS
	PiezoMUMPs
Teledyne DALSA	***MIDIS***



Front-side Bulk



SOIMUMPS



MIDIS™ cross section Dalsa

- Digressive prices are applied to most MPW services.
- Prices on the Web site.

Partnership:

Mar-18

Packaging for Prototyping & Low Volume Production

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CMP offers a wide variety of standard packages and assembly services for prototyping and low volume production.
Before starting a design, an important step is to select a package and/or packaging technic. Die package compatibility optimization can significantly impact the overall system performances.

Standard packaging

Complete assembly service based on a wide range of ceramic and plastic packages for prototyping and low volume production. Die pad ring compatibility with package cavity to be checked before sending your design.

Ceramic: ***CQFP, DIL, LCC, JLCC, PGA, SOIC, QFN…***

Plastic: ***BGA, QFN, QFP, PLCC, SOIC, TSSOP…***

Contact us

Jean-Francois PAILLOTIN [Jean-Francois.Paillotin@mycmp.fr]
Azedine MANAA [Azedine.Manaa@mycmp.fr]

Advanced packaging

Designers are supported every step of the way, from the installation and use of the PDK 3D Add-on to the final assembly-level verifications of your 3D project, which requires a specific and individual follow-up.

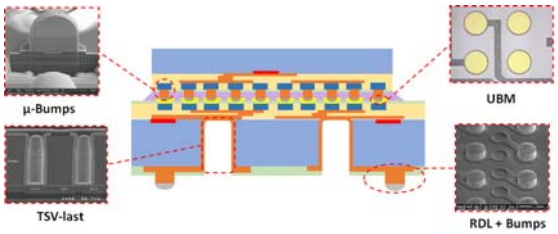
OPEN 3D post-processes in partnership with CEA/LETI in the frame of IRT Nanoelec
Set of post-processes allowing 3D interconnection integration at wafer-level, on various technology nodes after standard MPW & dedicated runs opened on STMicroelectronics **CMOS065, CMOS028FDSOI, BiCMOS055, BiCMOS9MW** and ams **C35B4M3.** MPW run opened once a year (check on the Web site).

- ***Front-side modules:*** µ-Bumps / UBM
- ***Back-side modules:*** TSV last + RDL + Bumps

Various types of assemblies supported :

- Single Die bumping for ***Flip-Chip packaging***
- ***Die-to-die*** stacking
- 2.5D integration on ***Silicon interposer.***

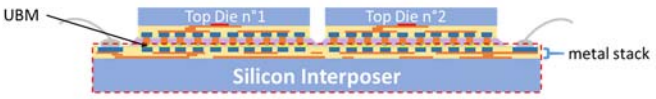
40 pieces delivered, prices available on the Website.



Silicon Interposer MPW runs in partnership with ams
2.5D Si-Interposer design and prototyping, support for dedicated assembly as an option.

- Both ***active*** (Frontend + Backend) and ***passive*** (Backend only) MPW runs are available
- Based on **ams C35** 4 layers metal stack (3 + 1 Thick)
- ***UBM*** deposited at wafer level (Ni/Pd/Au).

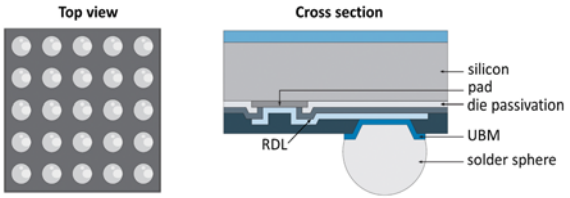
40 pieces delivered, prices available on the Website.



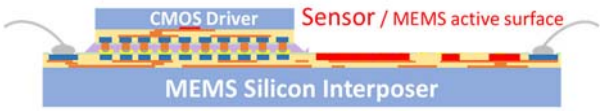
new **Wafer-level bumping** In partnership with ams
Wafer-level bumping service, manufactured on any ams 0.35 and 0.18µm MPW runs.
Supported in ams hitkit through an Add-on.

- Evenly ***distributed array*** over chip surface
- Electrical connections to CMOS pads with ***RDL layer***
- I/O Pitch compatible to ***PCB assembly processes .***

Price available on the website.



Hybrid packaging MEMS /Si Photonic + CMOS
Optical resin , Chip On Board (COB), Thermal solutions, Metallic package, Hermetic sealing.



- Prices on the Web site.

Contact us

Olivier GUILLER [olivier.guiller@mycmp.fr]
Lyubomir KERACHEV [lyubomir.kerachev@mycmp.fr]

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