

MPW prices



Prices are in Euro, valid for MPW runs starting after 1st January 2019. Price per mm² of the current price list is for 25 bare dies except for MEMSCAP, Open 3D, Teledyne DALSA. For STMicroelectronics and ams technologies 15 additional dies will be added free of charge when available. Beyond this quantity, dies are charged. Prices exclusive of taxes and duties and can be changed at any time without prior notice.

STANDARD price= normal price. **DISCOUNTED** price= only applies to EURO PRACTICE MEMBERS registered (who paid their annual full membership fee) Academic and Research Members from all 28 EU countries and Albania, Armenia, Azerbaijan, Belarus, Bosnia-Herzegovina, Georgia, Iceland, Israel, Liechtenstein, Former Yugoslav Republic of Macedonia, Moldova, Montenegro, Norway, Russia, Switzerland, Turkey, Serbia and Ukraine who submit designs for **educational or publicly funded research use only**. Prices are given for the delivery of unpackaged, untested prototypes. Packaging and testing will be charged separately.

DRC

Prices include DRC checking made by CMP before fabrication. In case of DRC errors CMP will contact you for corrections. Send your circuit layout before the deadline to have time for corrections.

Additional circuits

Few hundred parts: could be ordered at any time if available.
For more quantity: the order can only be made before the manufacturing deadline

Colour plots

Colour plots of the design can be ordered. Default format is around A0 (115cm x 76cm). Price per unit: 40€. Additional copy: 25€.

CMOS/BiCMOS/SiGe Integrated Circuits

ams ¹	STANDARD €/mm ²	DISCOUNTED price €/mm ²
ams 0.35µm CMOS C35B4C3 4M/2P/HR/5V IO	640 ²	580 ²
ams 0.35µm CMOS C35OPTO 4M/2P/5V IO	800 ³	700 ³
ams 0.35µm HV CMOS H35B4D3 120V 4M	880 ³	800 ³
ams 0.35µm SiGe-BiCMOS S35D4M5/CMOS-RF C35B4M3 4M/4P-MIM	880 ³	800 ³

Notes:

- ¹ Area = X*Y including seal-ring.
- ² Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 4 mm²
- ³ Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 7 mm²

Minimum charge

For each design, depending on the technology, a minimum surface, including seal-ring, is charged.

Shipment fees

Depending on destination, shipment fees for packaged circuits and bare dies are charged from 60€ up to 350€. For packaging services out a regular MPW (=external project or new packaging request on existing dies) shipment fees to and from packaging subcontractors are applied.

STMicroelectronics ¹	STANDARD €/mm ²	DISCOUNT €/project
ST 28nm CMOS28FDSOI	12000 ^{2,7} 24000+[(Area-2) x 9000] ⁵	1500
ST 55nm BiCMOS055	7500 ² 15000+[(Area-2) x 6000] ⁵	1200
ST 65nm CMOS065	6000 ³ 30000+[(Area-5) x 4900] ⁶	1200
ST 130nm BiCMOS9MW	2900 ³ 14500+[(Area-5) x 2400] ⁶	1000
ST 130nm H9SOI-FEM	2200 ³ 11000+[(Area-5) x 1500] ⁶	700
ST 130nm HCMOS9GP	2500 ³ 12500+[(Area-5) x 2200] ⁶	700
ST 130nm HCMOS9A	2500 ³ 12500+[(Area-5) x 2200] ⁶	700
ST 0.16µm BCD8sP	2500 ⁴ 12500+[(Area-5) x 2200] ⁶	1000
ST 0.16µm BCD8s-SOI	2500 ⁴ 12500+[(Area-5) x 2200] ⁶	1000
STMicroelectronics Wafer Level Bumping	STANDARD €/ project	DISCOUNT €/project
on 300mm ST 55nm BiCMOS055 process	25000	1500
on 300mm ST 65nm CMOS065	23000	1500
on 300mm ST 28nm CMOS28FDSOI	33000	1500

Notes:

- ¹ Area = X*Y including seal-ring.
- ² Price for Area ≤ 2mm² with minimum charge of 1.25mm² including seal-ring.
- ³ Price for Area ≤ 5mm² with minimum charge of 1.25mm² including seal-ring.
- ⁴ Price for Area ≤ 5mm² with minimum charge of 3.43mm² including seal-ring.
- ⁵ Price for 2mm² ≤ Area ≤ 10mm² including seal-ring. Contact CMP when Area is larger.
- ⁶ Price for 5mm² ≤ Area ≤ 15mm² including seal-ring. Contact CMP when Area is larger.
- ⁷ Special price for CNRS Institutions not cumulative with other offers: 9000€/mm²

OxRAM NVM and Si-Photonic processes

<i>IRT Nanoelec - LETI-CEA</i> ¹	STANDARD €/mm ²	DISCOUNT €/project
Non-volatile Memory (NVM) Silicon OxRAM 200mm (MAD200)	4000 ² 20000+[(Area-5) x 3200] ³	1200

Notes:
¹ Area = X*Y including seal-ring.
² Price for Area ≤ 5mm² with minimum charge of 3.43mm² including seal-ring.
³ Price for 5mm² ≤ Area ≤ 15mm² including seal-ring. Contact CMP when Area is larger.

<i>IRT Nanoelec - LETI-CEA</i> ¹	STANDARD €/mm ²	DISCOUNT €/project
Silicon Photonic Si310-PHMP2M	1600 ^{2,3} 16000 + (900/mm ²) ^{2,4}	700

Notes:
¹ Charged Area = multiples of 2mm² blocks including seal-ring.
² Each block is multiple 1 x 2 mm² and/or 2 x 1 mm²
³ Price for Area ≤ 10mm² with minimum charge of 2 blocks or 4 mm²
⁴ Price for additional blocks above 10mm² with minimum charge of 16000€.

Micro Electro Mechanical Systems - MEMS

<i>MEMSCAP</i>	STANDARD €/project	DISCOUNTED price €/project
PolyMUMPs, SOIMUMPs, PiezoMUMPs	3550 ¹	3350

Note:
¹ Fixed size 10x10mm

<i>ams</i>	STANDARD €/project	DISCOUNT €/project
ams 0.35µm CMOS Bulk Micromachining Front-side & Back-side for 10 prototypes	price under request	500

Wafer Level Die Preparation for Flip-chip Packaging

<i>IRT Nanoelec - LETI-CEA</i>	STANDARD €/project	DISCOUNT €/project
OPEN 3D µ-bumps (copper-pillars) Front-side µ-Bumps (copper-pillars) or UBM See "OPEN 3D post processes"	17000 ¹ 51300 ²	1500
Solder bumping post process on any project ³		
Gold stud-bumping on any project	1200 ⁴	200

Notes:
¹ MPW price
² Dedicated post process run
³ On quotation only (design dependant)
⁴ Price per design for 10 delivered pieces.

<i>ams</i>	STANDARD €/project	DISCOUNT €/project
Wafer-level bumping option on ams 0.35µm runs	6200 ¹	200

Notes:
¹ design for 40 delivered pieces.

Wafer level Advanced Packaging

<i>IRT Nanoelec - LETI-CEA</i> ¹	STANDARD €/project	DISCOUNT €/project
OPEN 3D post processes front-side only : µ-Bumps (copper-pillars) or UBM	MPW: 17000 Dedicated: 51300	1500
OPEN 3D post processes back-side only: TSV, RDL and Bumps	MPW: 55000 ²	2500
OPEN 3D post processes full: front-side + back-side	MPW: 72000 ²	4000

Notes:
¹ Open 3D post processes are available as MPW on the last runs of the year for the following technologies: C35B4M3 from ams, BiCMOS9MW, BiCMOS055, CMOS065 and CMOS28FDSOI (front-side only) from STMicroelectronics. OPEN 3D post-process MPW runs are subject to a sufficient level of participation. Guaranteed minimum delivered pieces 40.
² Additional fee participation for wafer sourcing.

Interposer Services

<i>ams</i>	STANDARD €/project	DISCOUNT €/project
0.35µm Active Silicon Interposer with UBM 3M+1TM ^{1,2} Interposer	50000 ³ 64000 ⁴	2500
Passive Silicon Interposer with UBM 3M+1TM ^{1,2} Interposer (<i>Backend only</i>)	40000 ⁵	2500

Notes:
¹ 3M+1TM: stack of 3 layers of metal and 4th Thick Top Metal.
² Guaranteed minimum delivered pieces 40
³ Price if Area < 100mm²
⁴ If 100mm²<Area <200mm²
⁵ For Area < 300mm² - For Area >300mm²: contact CMP

Standard packaging information and prices

Packaging is an important issue not to be neglected for the complete success of a prototype production and implementation. The first step before starting a design is to select a package. Pad ring has to match with cavity of the selected package to optimize the whole interconnection. If the pad ring is not correct you will have to buy a dedicated package, this is time consuming and price can be significantly higher than price of silicon. General assembly rules and common errors are available on mycmp.fr. A die ratio between 1 and 1.2 is recommended. Packaging should be ordered via the CMP Order Form before the deadline of the run. The bonding diagram should be sent with the CMP Order Form. Please check on our website for technical constraints on pad ring and for the price list and possible additional fees.

Wire-bond packaging process flow for MPW runs

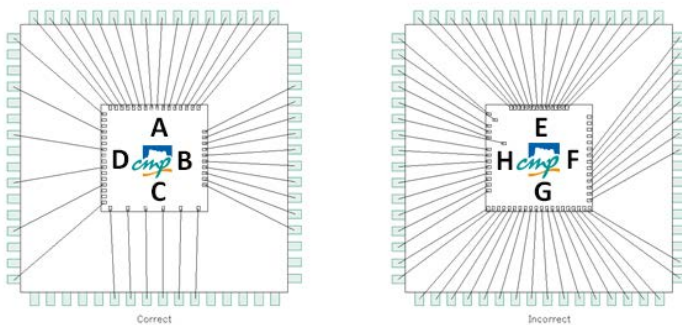
CMP offers a complete assembly service based on a wide range of ceramic and plastic packages for prototyping and low volume production.

Packaging guidelines

Prototypes packaging is a hard issue and yield can't be guaranteed. The pad ring of the circuit have to match with the selected package to optimize the number of good samples. When you request bonding of additional circuits after runs you have to provide us with 5 additional dies for setup of the bonding machine. These dies can be damaged by setup.

At least the following simple rules have to be followed for prototypes in ceramic packages. They are not strong enough for low volume production:

- Bonding pads have to be connected to the side of the package that is facing.
- Use a homogenous spacing for pads with the first pad and the last pad near corners.
- Use the biggest width of bonding pad compatible with the number of pad in a side.
- All bonding pads should have the same size and are perfectly aligned along circuit edges.
- Bonding pad structure has to be strong enough to avoid stretch off when bonding wires.
- No bonding pad in corners.
- Avoid long wires. Check with us for wires longer than 4500µm.
- Angles of wires with the circuit edge have to be between 45° and 90°.
- A bonding wire can't cross another bonding wire (this generates a shortcut).



- A:** the best configurations.
- B, C:** good configurations when the number of pads is smaller.
- D:** dummy pads are correctly inserted.
- E:** pads are concentrated in the middle of the circuit's side.
- F:** dummy pads are concentrated on top (long wires and acute angles).
- G:** too many pads, pads in the corner, the 2 first pads and the 2 last pads are not connected to the package side that is facing.
- H:** pads are not aligned.

The diameter of wires used for a circuit depend on size of the smallest pad of the circuit and on type of bonding (ball bonding or wedge bonding).

Some factors that are reducing yield:

- Long wire (shorts with neighbouring wires or with package cavity)
- Small pads (thin diameter for wires, risk to stretch wires off pads)
- Acute angles between wire and circuit edge (< 45°, shorts)
- Pads not perfectly aligned along the circuit edge (shorts)
- Pads incorrectly distributed in a side of the circuit (shorts)
- Bad bonding-pad structure (pad destroyed by bonding)
- Bonding pads in corners (generation of cracks on die)
- Big circuit ratio, length/width > 1.8 (long wires + acute angles)

Packaging service prices

- **Bonding diagram preparation fees**
 - A 100€ is applied for each packaging project + 50€ for each similar additional bonding diagram.
 - No fee for EP members.
- **Additional service fees**
 - 100€ for **packaging** on a CMP circuit when requested outside the MPW run progress.
 - 200€ for packaging of an IC **not fabricated through CMP**.
- **Packaging house set up fees**
 - for 40µm to 50µm pad size: 400€
 - for 51µm to 60µm pad size: 300€
 - for 61µm to 75µm pad size: 200€
 - for pad size >76µm: 200€ only for CQFPs and for QFNs.

In all cases, **a minimum of five (5)** packages per bonding diagram has to be ordered. For low volume packaging service, please contact us for a specific quotation. Prices may change without notice, check regularly mycmp.fr

Available standard package types and prices

CMP offers a complete assembly service based on a wide range of ceramic and plastic packages for prototyping and low volume production.

Types & associated services		Relevant features	Price in Euro per unit	
Small Outline (SOIC) 	Ceramic	Surface-mount device, rectangular, with smaller outline compared to a DIL package.	SOIC8: 70 SOIC16: 73 SOIC20: 83	SOIC24: 86 SOIC28: 90
C-leadless Chip Carriers (CLCC) 	Ceramic	Square surface-mount ceramic package with noleads. Flat metal contacts are on the 4 sides of the package bottom.	CLCC16: 44 CLCC20: 46 CLCC28: 48 CLCC32: 51	CLCC44: 58 CLCC48: 62 CLCC68: 79 CLCC84: 80
J-Leaded Chip Carriers (JLCC) 	Ceramic/Plastic	Square surface-mount ceramic package with J-formed leads around its periphery. The compatible plastic equivalent is PLCC	JLCC28: 71 JLCC44: 76 JLCC52: 83	JLCC68: 87 JLCC84: 99
Dual-in-line (DIL) 	Ceramic	DIL package is one of the most mature IC packages. It is rectangular with extended leads on the 2 long sides. (Not recommended for RF or high speed applications).	DIL8: 34 DIL14: 36 DIL16: 38 DIL18: 58 DIL20: 39	DIL24: 53 DIL28: 54 DIL40: 59 DIL48: 67
CerQuad Flat Pack (CQFP) 	Ceramic	Up to 256 I/Os Available options for pins: - Z: gull wing - J: Jleaded - F: Flat. Default option is pins bent in gull wing.	CQFP20J: 56 CQFP44ZJF: 75 CQFP64ZJF: 92 CQFP68JF: 88 CQFP80Z: 91 CQFP84J: 92 CQFP100ZF: 113	CQFP120Z: 123 CQFP128Z: 125 CQFP144Z: 133 CQFP160Z: 141 CQFP208Z: 176 CQFP240Z: 248 CQFP256Z: 260
Pin Grid Arrays (PGA) 	Ceramic	Up to 256 pins (up to 352 pins on request).	PGA68: 70 PGA84: 85 PGA100: 97 PGA120: 108 PGA144: 116	PGA160: 126 PGA180: 138 PGA208: 185 PGA224: 222 PGA256: 239
Thin Quad Flat Pad (TQFP) 	Plastic open cavity	25 samples minimum. These packages need thinned dies to 250µm, lids must be sealed.	TQFP32: 57 TQFP44: 64	TQFP52: 72 TQFP64: 80
Quad Flat Non Leaded (Open Cavity QFN) 	Plastic open cavity	Thermal performance, low inductance, high frequency. These packages need thinned dies to 250µm.	QFN12: 49 QFN16: 50 QFN20: 54 QFN24: 62 QFN28: 61 QFN32: 73 QFN36: 75 QFN40: 76	QFN44: 78 QFN48: 80 QFN52: 83 QFN56: 86 QFN64: 98 QFN80: 107 QFN88: 118 QFN100: 131
Plastic Open Cavity Packages	Plastic	Allows a smooth transfer between ceramic and plastic package (QFN, QFP, PLCC, PGA, BGA). 	Upon request	
Optical resin ¹ Chip On Board (COB) ² Thermal solutions ³ Metallic & Hermetic package ⁴		¹ Transparent, clear glob top and optical adhesive. ² Direct bonding of dies on organic substrates. ³ Thermal solutions: QFN, SFP, TQFP could be asked with Exposed Pad as an embedded heat sink. ⁴ For some applications (MEMS), it is possible to ask for hermetic sealing of ceramic packages.	Upon request	
Wafer level thinning		ams 0.35µm (8"): standard thinning to 530µm. ams 0.35µm (8"): thinning to 250µm on request STMicroelectronics 130nm (8"): standard thinning to 375µm.	Free of charge	
Die level thinning		Down to 150µm (absolute limit 100 µm)	Area < 1mm ² : 10€/die 1mm ² < Area < 5mm ² : 13€/die 5mm ² < Area < 10mm ² : 16€/die 10mm ² < Area < 15mm ² : 20€/die 15mm ² < Area contact CMP	
DRIE dicing	Option of thinning to 50µm	Clean borders of the chips, a better precision than conventional dicing	Upon request	