## MPW prices

Price per mm² of the current price list is for 25 bare dies except for MEMSCAP, Open 3D, Teledyne DALSA. For ST and ams technologies 15 additional dies will be added free of charge when available. Additional dies are charged.

## DRC

Prices include DRC checking made by CMP before fabrication. In case of DRC errors CMP will contact you for corrections. Send your circuit layout before the deadline to have time for corrections.

## Charged area

There is a minimum charge for each circuit depending on the technology considered for the design. This charge is defined as a minimum area. Excepted for MEMSCAP the charged area includes a seal ring of 60μm added by CMP around the circuit (120μm added in X and in Y axis).

**Examples for circuits in C35B4C3 technology of ams:**

➢ The circuit size is 1500μm x 1600μm (dimensions withor without the seal ring), you are charged the minimum area, 3.43mm² (including seal-ring). 3.43mm² * 650€/mm² = 2230€.

➢ The circuit size is 3000μm x 3000μm (limit of pad ring), you are charged the following surface: (3000μm + 120μm)*(3000μm + 120μm) = 9.73mm². 9.73mm² * 650€/mm² = 6325€.

### Additional circuits

Low volume (<100) of additional circuits can be ordered at any time as a function of availabilities. Larger volume (>300) of additional circuits must be ordered before the deadline for manufacture. Contact CMP for precise estimates. Prices are determined on a case per case basis.

### Colour plots

Colour plots of the design can be ordered. Default format is around A0 (115cm x 76cm). Price: 40€ for the first sample and 25€ per copy.

### Shipment fees

Depending on destination, shipment fees for circuits and packaging are charged from 60€ up to 350€. For packaging services out a regular MPW (=external project or new packaging request on existing dies) shipment fees to and from packaging subcontractors are applied.

**Prices are exclusive of taxes and duties and can be changed at any time without prior notice.**

A minimum charge apply on most MPW services (invoice of a minimum surface).

## CMOS/BiCMOS/SiGe Integrated Circuits

| **ams** (1) | | - For very large circuits: specific quotation under request - | |
|---|---|---|---|
| 0.18μm | CMOS C18A6 | 1200€/mm² (2) | *if Area less or equal to 10mm²* |
| | | 12000€ + [(Area-10) x 1100€] | *if Area > 10mm²* |
| 0.18μm | HV-CMOS H18A6 | 1200€/mm² (2) | *if Area less or equal to 10mm²* |
| | | 12000€ + [(Area-10) x 1100€] | *if Area > 10mm²* |
| 0.35μm | CMOS C35B4C3 | 650€/mm² (3) | *if Area less or equal to 10mm²* |
| | | 6500€ + [(Area-10) x 550€] | *if Area > 10mm²* |
| 0.35μm | CMOS-RF C35B4M3 | 950€/mm² (4) | *if Area less or equal to 10mm²* |
| | | 9500€ + [(Area-10) x 850€] | *if Area > 10mm²* |
| 0.35μm | CMOS-Opto BARC C35B40A | 650€/mm² (3) | *if Area less or equal to 10mm²* |
| | | 6500€ + [(Area-10) x 550€] | *if Area > 10mm²* |
| | | + fixed fee 6900€ | |
| 0.35μm | CMOS-Opto ARC C35B40I | 700€/mm² (3) | *if Area less or equal to 10mm²* |
| | | 7000€ + [(Area-10) x 600€] | *if Area > 10mm²* |
| 0.35μm | SiGe BiCMOS S35D4M5 | 950€/mm² (4) | *if Area less or equal to 10mm²* |
| | | 9500€ + [(Area-10) x 850€] | *if Area > 10mm²* |
| 0.35μm | C35B4E3 | Available upon request with additional fees. | |
| 0.35μm | HV-CMOS H35B4D3 | 850€/mm² (5) | *if Area less or equal to 10mm²* |
| | | 8500€ + [(Area-10) x 750€] | *if Area > 10mm²* |
| 0.35μm | MEMS CMOS Bulk Micromachining Front-side & Back-side | price under request | |
| **STMicroelectronics** (1) | | | |
| 28nm | FDSOI CMOS28FDSOI | 12000€/mm² (6) | *if Area less or equal to 2mm²* |
| | | Special price for CNRS Institutions: 9000€/mm² (6) | |
| | | 24000€ + [(Area-2) x 9000€] | *if 2mm² < Area < 10mm²(7)* |
| 55nm | SiGe BiCMOS055 | 7500€/mm² (6) | *if Area less or equal to 2mm²* |
| | | 15000€ + [(Area-2) x 6000€] | *if 2mm² < Area < 10mm²(7)* |
| 65nm | CMOS CMOS065 | 6000€/mm² (6) | *if Area less or equal to 5mm²* |
| | | 30000€ + [(Area-5) x 4900€] | *if 5mm² < Area < 15mm²(7)* |
| 130nm | CMOS HCMOS9GP | 2500€/mm² (6) | *if Area less or equal to 5mm²* |
| | | 12500€ + [(Area-5) x 2200€] | *if 5mm² < Area < 15mm² (7)* |
| 130nm | SiGe BiCMOS9MW | 2900€/mm² (6) | *if Area less or equal to 5mm²* |
| | | 14500€ + [(Area-5) x 2400€] | *if 5mm² < Area < 15mm² (7)* |
| 130nm | SOI H9SOI-FEM | 2200€/mm² (6) | *if Area less or equal to 5mm²* |
| | | 11000€ + [(Area-5) x 1500€] | *if 5mm² < Area < 15mm² (7)* |
| 130nm | CMOS HCMOS9A | 2500€/mm² (6) | *if Area less or equal to 5mm²* |
| | | 12500€ + [(Area-5) x 2200€] | *if 5mm² < Area < 15mm² (7)* |
| 0.16μm | BCD BCD8sP | 2500€/mm² (3) | *if Area less or equal to 5mm²* |
| | | 12500€ + [(Area-5) x 2200€] | *if 5mm² < Area < 15mm² (7)* |
| 0.16μm | BCD BCD8s-SOI | 2500€/mm² (3) | *if Area less or equal to 5mm²* |
| | | 12500€ + [(Area-5) x 2200€] | *if 5mm² < Area < 15mm² (7)* |

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## Silicon Photonic Integrated Circuits

### IRT Nanoelec - LETI-CEA (1)

| | | | |
|---|---|---|---|
| | Si310-PHMP2M | 3200€/block ->Each block is 2x1mm² or 1x2mm² (15) | *if Area less or equal to 10mm² and* |
| | | 1800€/block ->Each block is 2x1mm² or 1x2mm² (16) | *for additional blocks above 10mm².* |

## Non-Volatile Memory (NVM) Integrated Circuits

*new* ### IRT Nanoelec - LETI-CEA (1)

| | | | |
|---|---|---|---|
| | Memory Advanced Demonstrator **Silicon OxRAM** 200mm (MAD200) | 4000€/mm² (3) | *if Area less or equal to 5mm²* |
| | | 20000€ + [(Area-5) x 3200€] | *if 5mm² < Area < 15mm² (7)* |

## Micro Electro Mechanical Systems - MEMS

### MEMSCAP

| | | | |
|---|---|---|---|
| | PolyMUMPs | 3900€ (8) (9) (10) (13) | 4600€ (11) (9) (10) (13) |
| | PiezoMUMPs | 3900€ (8) (10) (13) | 4600€ (11) (10) (13) |
| | SOIMUMPs | 3900€ (8) (9) (10) (14) | 4600€ (12) (9) (10) (14) |

### ams (1)

| | | |
|---|---|---|
| | 0.35µm CMOS Bulk Micromachining Front-side & Back-side | price under request |

## Wafer Level Die Preparation for Flip-chip Packaging

### IRT Nanoelec - LETI-CEA

| | | |
|---|---|---|
| | OPEN 3D µ-bumps (copper-pillars) Front-side µ-Bumps (copper-pillars) or UBM *See "OPEN 3D post processes"* | As MPW : 17000€ As Dedicated post process run: 51300€ |
| | Solder bumping post process on any project | On quotation only (design dependant) |
| | Gold stud-bumping on any project | 1200€ *per design for 10 delivered pieces* |

### ams

| | | |
|---|---|---|
| | Wafer-level bumping option on ams 0.35µm & 0.18µm runs | 6200€ *per design for 40 delivered pieces* |

## Wafer level Advanced Packaging

### IRT Nanoelec - LETI-CEA

| | | |
|---|---|---|
| | OPEN 3D post processes front-side only : µ-Bumps (copper-pillars) or UBM | As MPW : 17000 € As Dedicated post process run: 51300€ |
| | OPEN 3D post processes back-side only: TSV, RDL and Bumps | As MPW : 55000 € + fee participation for wafer sourcing As Dedicated post process run: *contact CMP* |
| | OPEN 3D post processes full: front-side + back-side | As MPW : 72000 € + fee participation for wafer sourcing As Dedicated post process run: *contact CMP* |

Open 3D post processes are available as MPW on the last runs of the year for the following technologies: C35B4M3 from ams, BiCMOS9MW, BiCMOS055, CMOS065 and CMOS28FDSOI (front-side only) from STMicroelectronics. OPEN 3D post-process MPW runs are subject to a sufficient level of participation. Guaranteed minimum delivered pieces 40

## Interposer Services

*new* ### ams

| | | | |
|---|---|---|---|
| | 0.35µm Active Silicon Interposer with UBM 3M+1TM** interposer *Guaranteed minimum delivered pieces 40* | 50000€ | *if Area < 100mm²* |
| | | 64000€ | *if Area < 100mm²* |
| | Passive Silicon Interposer with UBM 3M+1TM** interposer (*Backend only*) *Guaranteed minimum delivered pieces 40* | 40000€ | *For Area < 300mm²* |
| | | *For Area >300mm²: contact CMP* | |

** 3M+1TM: stack of 3 layers of metal and 4th Thick Top Metal.

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1. Area = (X + 0.12) * (Y + 0.12) mm².
2. Minimum charge is the price of 5.55mm² (X+0.12)*(Y+0.12)mm².
3. Minimum charge is the price of 3.43mm² (X+0.12)*(Y+0.12)mm².
4. Minimum charge is the price of 4.49mm² (X+0.12)*(Y+0.12)mm².
5. Minimum charge is the price of 7.65mm² (X+0.12)*(Y+0.12)mm².
6. Minimum charge is the price of 1.25mm² (X+0.12)*(Y+0.12)mm².
7. Contact CMP for a price quotation when Area is larger.
8. Price for Educational Institutions and Research Labs.
9. Additional prices for Subdicing and Release:
   - Subdicing: 220€ per cut lane and per 15 chips,
   - HF Release: 870€ flat rate for up to 60 die/subdie,
   - Supercritical CO2 Dry: 1100€ flat rate for up to 60 die/subdie.

10. Contact CMP for multiple location prices.
11. Price for Industrial Companies.
12. Fixed size.
13. For 15 identical chips, 1cm x 1cm (fixed size).
14. For 15 identical chips 0.9cm x 0.9cm (fixed size).
15. Minimum charge is the price of 2 blocs or 4mm².
16. Minimum charge is 16000€.
17. Minimum charge is the price of 3.00mm² (X+0.12)*(Y+0.12) mm².

## Die Level Standard Packaging Information and Prices

Packaging is an important issue not to be neglected for the complete succes of a prototype production and implementation. The first step before starting a design is to select a package. Pad ring has to match with cavity of the selected package to optimize the whole interconnection. If the pad ring is not correct you will have to buy a dedicated package, this is time consuming and price can be significantly higher than price of silicon. General assembly rules and common errors are available on the web site.

A die ratio between 1 and 1.2 is recommended. Packaging should be ordered via the CMP Order Form before the deadline of the run. The bonding diagram should be sent with the CMP Order Form. Please check on our website for technical constraints on pad ring and for the price list and possible additional fees.

### Wire-bond packaging process flow for MPW runs

CMP offers a complete assembly service based on a wide range of ceramic and plastic packages for prototyping and low volume production.

### Packaging guidelines

Prototypes packaging is a hard issue and yield can't be guaranteed. The pad ring of the circuit have to match with the selected package to optimize the number of good samples. When you request bonding of additional circuits after runs you have to provide us with 5 additional dies for setup of the bonding machine. These dies can be damaged by setup.

At least the following simple rules have to be followed for prototypes in ceramic packages. They are not strong enough for low volume production:

- Bonding pads have to be connected to the side of the package that is facing.
- Use a homogenous spacing for pads with the first pad and the last pad near corners.
- Use the biggest width of bonding pad compatible with the number of pad in a side.
- All bonding pads should have the same size and are perfectly aligned along circuit edges.
- Bonding pad structure has to be strong enough to avoid stretch off when bonding wires.
- No bonding pad in corners.
- Avoid long wires. Check with us for wires longer than 4500µm.
- Angles of wires with the circuit edge have to be between 45° and 90°.
- A bonding wire can't cross another bonding wire (this generates a shortcut).
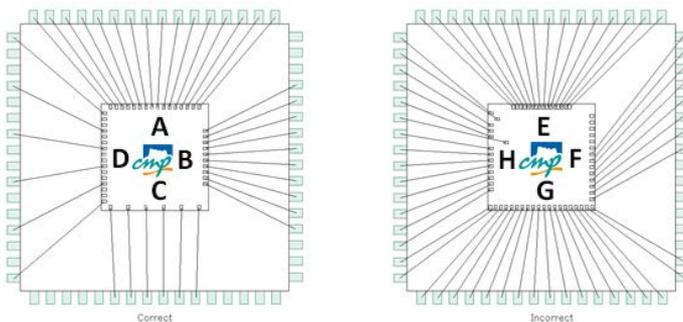


**A:** the best configurations.
**B, C:** good configurations when the number of pads is smaller.
**D:** dummy pads are correctly inserted.
**E:** pads are concentrated in the middle of the circuit's side.
**F:** dummy pads are concentrated on top (long wires and acute angles).
**G:** too many pads, pads in the corner, the 2 first pads and the 2 last pads are not connected to the package side that is facing.
**H:** pads are not aligned.

The diameter of wires used for a circuit depend on size of the smallest pad of the circuit and on type of bonding (ball bonding or wedge bonding).

Some factors that are reducing yield:

- Long wire (shorts with neighbouring wires or with package cavity)
- Small pads (thin diameter for wires, risk to stretch wires off pads)
- Acute angles between wire and circuit edge ($< 45°$, shorts)
- Pads not perfectly aligned along the circuit edge (shorts)
- Pads incorrectly distributed in a side of the circuit (shorts)
- Bad bonding-pad structure (pad destroyed by bonding)
- Bonding pads in corners (generation of cracks on die)
- Big circuit ratio, length/width $> 1.8$ (long wires + acute angles)

## Available standard package types and associated services:

- A 100€ **wiring plan preparation fees** is applied for each packaging project + 50€ for each additional bonding diagram on the same.
- An additional 200€ service fee is applied for **packaging** on a CMP circuit when requested outside the MPW run progress.
- An additional 500€ service fee is applied for packaging of an IC **not fabricated through CMP**:

Depending on IC pad size, additional **set up fee is applied for each bonding diagram**:
- for 40µm to 50µm pad size: 384€
- for 51µm to 60µm pad size: 288€
- for 61µm to 75µm pad size: 192€
- for pad size >76µm: 192€ for CQFPs and for QFNs, no additional fee for other standard packages.

In all cases, **a minimum of five (5)** packages per bonding diagram has to be ordered.
Additional bonding wires can be charged. Price is quoted on a case per case basis for circuits with long wires. Note that five (5) bare dies are requested for set-up of the bonding machine.
For small volume packaging service, please contact us for a specific quotation.

| Types & associated services | Relevant features | Price per unit | |
|---|---|---|---|
| **Small Outline (SOIC)** | Ceramic | SOIC8: 66.50€<br>SOIC16: 68.40€<br>SOIC20: 78.95€ | SOIC24: 81.95€<br>SOIC28: 85.70€ |
| **C-leadless Chip Carriers (CLCC)** | Ceramic | CLCC16: 40.45€<br>CLCC20: 42.25€<br>CLCC28: 43.70€<br>CLCC32: 46.70€ | CLCC44: 52.90€<br>CLCC48: 57.25€<br>CLCC68: 73.80€<br>CLCC84: 75.30€ |
| **J-Leaded Chip Carriers (JLCC)** | Ceramic/Plastic | JLCC28: 66.50€<br>JLCC44: 71.50€<br>JLCC52: 78.95€ | JLCC68: 81.96€<br>JLCC84: 95.15€ |
| **Dual-in-line (DIL)** | Ceramic | DIL8: 31.20€<br>DIL14: 32.40€<br>DIL16: 33.60€<br>DIL18: 52.70€<br>DIL20: 36.00€ | DIL24: 48.50€<br>DIL28: 53.60€<br>DIL40: 58.60€<br>DIL48: 62.15€ |
| **CerQuad Flat Pack (CQFP)** | Ceramic | Up to 256 I/Os<br>Available options for pins:<br>- Z: gull wing<br>- J: Jleaded<br>- F: Flat<br>Default option is pins bent in gull wing<br><br>CQFP20J: 54.10€<br>CQFP44ZJF: 72.70€<br>CQFP64ZJF: 88.30€<br>CQFP68JF: 85.90€<br>CQFP80Z: 88.75€<br>CQFP84J: 89.30€<br>CQFP100ZF: 110.20€ | CQFP120Z: 120.00€<br>CQFP128Z: 121.80€<br>CQFP144Z: 130.70€<br>CQFP160Z: 138.50€<br>CQFP208Z: 173.75€<br>CQFP240Z: 242.40€<br>CQFP256Z: 254.75€ |
| **Pin Grid Arrays (PGA)** | Ceramic | Up to 352 pins<br><br>PGA68: 68.40€<br>PGA84: 78.70€<br>PGA100: 93.00€<br>PGA120: 104.05€<br>PGA144: 112.55€ | PGA160: 123.60€<br>PGA180: 135.00€<br>PGA208: 183.05€<br>PGA224: 217.70€<br>PGA256: 238.55€ |
| **Thin Quad Flat Pad (TQFP)** | Plastic open cavity | 25 samples minimum<br>Theses packages need thinned dies, lids must be sealed<br><br>TQFP32: 53.30€<br>TQFP44: 60.70€ | TQFP52: 67.80€<br>TQFP64: 75.50€ |
| **Quad Flat Non Leaded (Open Cavity QFN)** | Plastic open cavity | Thermal performance, low inductance, high frequency<br>Theses packages need thinned dies<br><br>QFN12: 44.75€<br>QFN16: 44.75€<br>QFN24: 57.10€<br>QFN28: 57.10€<br>QFN32: 66.95€<br>QFN36: 70.70€<br>QFN40: 71.15€ | QFN44: 73.70€<br>QFN48: 75.60€<br>QFN52: 77.40€<br>QFN56: 80.40€<br>QFN64: 91.55€<br>QFN80: 102.70€ |
| **Plastic Open Cavity Packages** | Plastic | Allows a smooth transfer between ceramic and plastic pakage (QFN, QFP, PLCC, PGA, BGA) | *Upon request* | |
| **Optical resin, Chip On Board (COB), Thermal solutions, Metallic & Hermetic package** | | | *Upon request* | |
| **Wafer level thinning** | | ams 0.35 µm (8") : standard  thinning to 530µm<br>ams 0.35 µm (8") : thinning to 250 µm on request STMicroelectronics<br>130 nm (8") : standard  thinning to 375µm | *Free of charge* | |
| **Die level thinning** | | Down to 150 µm (absolute limit 100µm) | Area<1mm2:  10€/die<br>1mm2<Area<5mm2:       13€/die<br>5mm2<Area<10mm2:     16€/die<br>10mm2<Area<15mm2:     20€/die<br>15mm2< Area contact CMP | |
| **DRIE dicing** | Option of thinning to 50µm | Clean borders of the chips, a better precision than conventional dicing | *Upon request* | |

*Note:       Prices may change without notice, check regularly mycmp.fr*

Sept-18

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