Prices are in Euro, valid for MPW runs starting after 1st October 2019. Price per mm² of the current price list is for 25 bare dies except for MEMSCAP, Open 3D, Teledyne DALSA. For STMicorelectronics and ams technologies 15 additional dies will be added free of charge when available. Beyond this quantity, dies are charged. Prices exclusive of taxes and duties and can be changed at any time without prior notice.
**STANDARD** price= normal price. **DISCOUNTED** price= only applies to EUROPRACTICE MEMBERS registered (who paid their annual full membership fee) Academic and Research Members from all 28 EU countries and Albania, Armenia, Azerbaijan, Belarus, Bosnia-Herzegovina, Georgia, Iceland, Israel, Liechtenstein, Former Yugoslav Republic of Macedonia, Moldova, Montenegro, Norway, Russia, Switzerland, Turkey, Serbia and Ukraine who submit designs for **educational or publicly funded research use only**. Prices are given for the delivery of unpackaged, untested prototypes. Packaging and testing will be charged separately.

## DRC

Prices include DRC checking made by CMP before fabrication. In case of DRC errors CMP will contact you for corrections. Send your circuit layout before the deadline to have time for corrections.

## Additional circuits

Few hundred parts: could be ordered at any time if available.
For more quantity: the order can only be made before the manufacturing deadline

## Colour plots

Colour plots of the design can be ordered. Default format is around A0 (115cm x 76cm). Price per unit: 40€. Additional copy: 25€.

## Minimum charge

For each design, depending on the technology, a minimum surface, including seal-ring, is charged.

## Shipment fees

Depending on destination, shipment fees for packaged circuits and bare dies are charged from 60€ up to 350€. For packaging services out a regular MPW (=external project or new packaging request on existing dies) shipment fees to and from packaging subcontractors are applied.

**CMOS/BiCMOS/SiGe Integrated Circuits**

| *ams* [1] | STANDARD €/mm² | DISCOUNTED price €/mm² |
|---|---|---|
| ams 0.35µm CMOS C35B4C3 4M/2P/HR/5V IO | 640 [2] | 580 [2] |
| ams 0.35µm CMOS C35OPTO 4M/2P/5V IO | 800 [3] | 700 [3] |
| ams 0.35µm HV CMOS H35B4D3 120V 4M | 880 [2] | 800 [2] |
| ams 0.35µm SiGe-BiCMOS S35D4M5/CMOS-RF C35B4M3 4M/4P-MIM | 880 [2] | 800 [2] |

**Notes:**
[1] Area = X*Y including seal-ring.
[2] Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 7 mm²
[3] Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 20 mm²

| *STMicroelectronics* [1] | STANDARD €/mm² | DISCOUNT €/project |
|---|---|---|
| ST 28nm CMOS28FDSOI | 9000 [2,7]<br>18000+[(Area-2) x 6750] [5] | 1500 |
| ST 55nm BiCMOS055 | 5500 [2]<br>11000+[(Area-2) x 4250] [5] | 1200 |
| ST 65nm CMOS065 | 4500 [3]<br>22500+[(Area-5) x 3750] [6] | 1200 |
| ST 130nm BiCMOS9MW | 2600 [3]<br>13000+[(Area-5) x 2200] [6] | 1000 |
| ST 130nm H9SOI-FEM | 2200 [3]<br>11000+[(Area-5) x 1500] [6] | 700 |
| ST 130nm HCMOS9GP | 2500 [3]<br>12500+[(Area-5) x 2200] [6] | 700 |
| ST 130nm HCMOS9A | 2500 [3]<br>12500+[(Area-5) x 2200] [6] | 700 |
| ST 0.16µm BCD8sP | 2500 [4]<br>12500+[(Area-5) x 2200] [6] | 1000 |
| ST 0.16µm BCD8s-SOI | 2500 [4]<br>12500+[(Area-5) x 2200] [6] | 1000 |
| *STMicroelectronics Wafer Level Bumping* | **STANDARD €/ project** | **DISCOUNT €/project** |
| on 300mm ST 55nm BiCMOS055 process | 25000 | 1500 |
| on 300mm ST 65nm CMOS065 | 23000 | 1500 |
| on 300mm ST 28nm CMOS28FDSOI | 33000 | 1500 |

**Notes:**
[1] Area = X*Y including seal-ring.
[2] Price for Area ≤ 2mm² with minimum charge of 1.25mm² including seal-ring.
[3] Price for Area ≤ 5mm² with minimum charge of 1.25mm² including seal-ring.
[4] Price for Area ≤ 5mm² with minimum charge of 3.43mm² including seal-ring.
[5] Price for 2mm² ≤ Area ≤ 10mm² including seal-ring. Contact CMP when Area is larger.
[6] Price for 5mm² ≤ Area ≤ 15mm² including seal-ring. Contact CMP when Area is larger.
[7] Special additional discount for CNRS Institutions: 1500€/project.



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## OxRAM NVM and Si-Photonic processes

| IRT Nanoelec - LETI-CEA [1] | STANDARD €/mm² | DISCOUNT €/project |
| --- | --- | --- |
| Non-volatile Memory (NVM) Silicon OxRAM 200mm (MAD200) | 4000 [2]<br>20000+[(Area-5) x 3200] [3] | 1200 |

**Notes:**
[1] Area = X*Y including seal-ring.
[2] Price for Area ≤ 5mm² with minimum charge of 3.43mm² including seal-ring.
[3] Price for 5mm² ≤ Area ≤ 15mm² including seal-ring. Contact CMP when Area is larger.

| IRT Nanoelec - LETI-CEA [1] | STANDARD €/mm² | DISCOUNT €/project |
| --- | --- | --- |
| Silicon Photonic Si310-PHMP2M | 1600 [2,3]<br>16000 + (900/mm²) [2,4] | 700 |

**Notes:**
[1] Charged Area = multiples of 2mm² blocks including seal-ring.
[2] Each block is multiple 1 x 2 mm² and/or 2 x 1 mm²
[3] Price for Area ≤ 10mm² with minimum charge of 2 blocks or 4 mm²
[4] Price for additional blocks above 10mm² with minimum charge of 16000€.

## Micro Electro Mechanical Systems - MEMS

| MEMSCAP | STANDARD €/project | DISCOUNTED price €/project |
| --- | --- | --- |
| PolyMUMPs, SOIMUMPs, PiezoMUMPs | 3550 [1] | 3350 |

**Note:**
[1] Fixed size 10x10mm

| ams | STANDARD €/project | DISCOUNT €/project |
| --- | --- | --- |
| ams 0.35µm CMOS Bulk Micromachining<br>Front-side & Back-side for 10 prototypes | price under request | 500 |

## Wafer Level Die Preparation for Flip-chip Packaging

| IRT Nanoelec - LETI-CEA | STANDARD €/project | DISCOUNT €/project |
| --- | --- | --- |
| OPEN 3D µ-bumps (copper-pillars)<br>Front-side µ-Bumps (copper-pillars) or UBM<br>See "OPEN 3D post processes" | 17000 [1]<br>51300 [2] | 1500 |
| Solder bumping post process on any project [3] | | |
| Gold stud-bumping on any project | 1200 [4] | 200 |

**Notes:**
[1] MPW price
[2] Dedicated post process run
[3] On quotation only (design dependant)
[4] Price per design for 10 delivered pieces.

| ams | STANDARD €/project | DISCOUNT €/project |
| --- | --- | --- |
| Wafer-level bumping option on ams 0.35µm runs | 6200 [1] | 200 |

**Notes:**
[1] design for 40 delivered pieces.

## Wafer level Advanced Packaging

| IRT Nanoelec - LETI-CEA [1] | STANDARD €/project | DISCOUNT €/project |
| --- | --- | --- |
| OPEN 3D post processes front-side only : µ-Bumps (copper-pillars) or UBM | MPW: 17000<br>Dedicated: 51300 | 1500 |
| OPEN 3D post processes back-side only: TSV, RDL and Bumps | MPW: 55000 [2] | 2500 |
| OPEN 3D post processes full: front-side + back-side | MPW: 72000 [2] | 4000 |

**Notes:**
[1] Open 3D post processes are available as MPW on the last runs of the year for the following technologies: C35B4M3 from ams, BiCMOS9MW, BiCMOS055, CMOS065 and CMOS28FDSOI (front-side only) from STMicroelectronics. OPEN 3D post-process MPW runs are subject to a sufficient level of participation. Guaranteed minimum delivered pieces 40.
[2] Additional fee participation for wafer sourcing.

## Interposer Services

| ams | STANDARD €/project | DISCOUNT €/project |
| --- | --- | --- |
| 0.35µm Active Silicon Interposer with UBM 3M+1TM [1,2] Interposer | 50000 [3]<br>64000 [4] | 2500 |
| Passive Silicon Interposer with UBM 3M+1TM [1,2] Interposer (*Backend only*) | 40000 [5] | 2500 |

**Notes:**
[1] 3M+1TM: stack of 3 layers of metal and 4th Thick Top Metal.
[2] Guaranteed minimum delivered pieces 40
[3] Price if Area < 100mm²
[4] if 100mm²<Area <200mm²
[5] For Area < 300mm² - For Area >300mm²: contact CMP



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## Standard packaging information and prices

Packaging is an important issue not to be neglected for the complete succes of a prototype production and implementation. The first step before starting a design is to select a package. Pad ring has to match with cavity of the selected package to optimize the whole interconnection. If the pad ring is not correct you will have to buy a dedicated package, this is time consuming and price can be significantly higher than price of silicon. General assembly rules and common errors are available on mycmp.fr
A die ratio between 1 and 1.2 is recommanded. Packaging should be ordered via the CMP Order Form before the deadline of the run. The bonding diagram should be sent with the CMP Order Form. Please check on our website for technical constraints on pad ring and for the price list and possible additional fees.

### Wire-bond packaging process flow for MPW runs

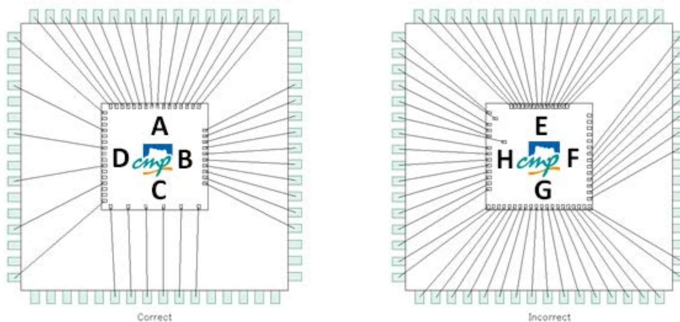
CMP offers a complete assembly service based on a wide range of ceramic and plastic packages for prototyping and low volume production.

### Packaging guidelines

Prototypes packaging is a hard issue and yield can't be guaranteed. The pad ring of the circuit have to match with the selected package to optimize the number of good samples. When you request bonding of additional circuits after runs you have to provide us with 5 additional dies for setup of the bonding machine. These dies can be damaged by setup.

At least the following simple rules have to be followed for prototypes in ceramic packages. They are not strong enough for low volume production:

- Bonding pads have to be connected to the side of the package that is facing.
- Use a homogenous spacing for pads with the first pad and the last pad near corners.
- Use the biggest width of bonding pad compatible with the number of pad in a side.
- All bonding pads should have the same size and are perfectly aligned along circuit edges.
- Bonding pad structure has to be strong enough to avoid stretch off when bonding wires.
- No bonding pad in corners.
- Avoid long wires. Check with us for wires longer than 4500µm.
- Angles of wires with the circuit edge have to be between 45° and 90°.
- A bonding wire can't cross another bonding wire (this generates a shortcut).




**A:** the best configurations.
**B, C:** good configurations when the number of pads is smaller.
**D:** dummy pads are correctly inserted.
**E:** pads are concentrated in the middle of the circuit's side.
**F:** dummy pads are concentrated on top (long wires and acute angles).
**G:** too many pads, pads in the corner, the 2 first pads and the 2 last pads are not connected to the package side that is facing.
**H:** pads are not aligned.

The diameter of wires used for a circuit depend on size of the smallest pad of the circuit and on type of bonding (ball bonding or wedge bonding).

Some factors that are reducing yield:

- Long wire (shorts with neighbouring wires or with package cavity)
- Small pads (thin diameter for wires, risk to stretch wires off pads)
- Acute angles between wire and circuit edge (< 45°, shorts)
- Pads not perfectly aligned along the circuit edge (shorts)
- Pads incorrectly distributed in a side of the circuit (shorts)
- Bad bonding-pad structure (pad destroyed by bonding)
- Bonding pads in corners (generation of cracks on die)
- Big circuit ratio, length/width > 1.8 (long wires + acute angles)

### Packaging service prices

- **Bonding diagram preparation fees**
  - A 100€ is applied for each packaging project + 50€ for each similar additional bonding diagram.
  - No fee for EP members.
- **Additonal service fees**
  - 100€ for **packaging** on a CMP circuit when requested outside the MPW run progress.
  - 200€ for packaging of an IC **not fabricated through CMP.**
- **Packaging house set up fees**
  - for 40µm to 50µm pad size: 400€
  - for 51µm to 60µm pad size: 300€
  - for 61µm to 75µm pad size: 200€
  - for pad size >76µm: 200€ only for CQFPs and for QFNs.

In all cases, **a minimum of five (5)** packages per bonding diagram has to be ordered.
For low volume packaging service, please contact us for a specific quotation.
Prices may change without notice, check regularly mycmp.fr



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## Available standard package types and prices

CMP offers a complete assembly service based on a wide range of ceramic and plastic packages for prototyping and low volume production.

| Types & associated services | | Relevant features | Price in Euro per unit | |
|---|---|---|---|---|
| **Small Outline (SOIC)** | Ceramic | Surface-mount device, rectangular, with smaller outline compared to a DIL package. | SOIC8: 70<br>SOIC16: 73<br>SOIC20: 83 | SOIC24: 86<br>SOIC28: 90 |
| **C-leadless Chip Carriers (CLCC)** | Ceramic | Square surface-mount ceramic package with noleads. Flat metal contacts are on the 4 sides of the package bottom. | CLCC16: 44<br>CLCC20: 46<br>CLCC28: 48<br>CLCC32: 51 | CLCC44: 58<br>CLCC48: 62<br>CLCC68: 79<br>CLCC84: 80 |
| **J-Leaded Chip Carriers (JLCC)** | Ceramic/Plastic | Square surface-mount ceramic package with J-formed leadsaround its periphery. The compatible plastic equivalent is PLCC | JLCC28: 71<br>JLCC44: 76<br>JLCC52: 83 | JLCC68: 87<br>JLCC84: 99 |
| **Dual-in-line (DIL)** | Ceramic | DIL package is one of the most mature IC pacakges. It is rectangular with extended leads on the 2 long sides. (Not recommended for RF or high speed applications). | DIL8: 34<br>DIL14: 36<br>DIL16: 38<br>DIL18: 58<br>DIL20: 39 | DIL24: 53<br>DIL28: 54<br>DIL40: 59<br>DIL48: 67 |
| **CerQuad Flat Pack (CQFP)** | Ceramic | Up to 256 I/Os<br>Available options for pins:<br>- Z: gull wing<br>- J: Jleaded<br>- F: Flat.<br>Default option is pins bent in gull wing. | CQFP20J: 56<br>CQFP44ZJF: 75<br>CQFP64ZJF: 92<br>CQFP68JF: 88<br>CQFP80Z: 91<br>CQFP84J: 92<br>CQFP100ZF: 113 | CQFP120Z: 123<br>CQFP128Z: 125<br>CQFP144Z: 133<br>CQFP160Z: 141<br>CQFP208Z: 176<br>CQFP240Z: 248<br>CQFP256Z: 260 |
| **Pin Grid Arrays (PGA)** | Ceramic | Up to 256 pins (up to 352 pins on request). | PGA68: 70<br>PGA84: 85<br>PGA100: 97<br>PGA120: 108<br>PGA144: 116 | PGA160: 126<br>PGA180: 138<br>PGA208: 185<br>PGA224: 222<br>PGA256: 239 |
| **Thin Quad Flat Pad (TQFP)** | Plastic open cavity | 25 samples minimum.<br>Theses packages need thinned dies to 250µm, lids must be sealed. | TQFP32: 57<br>TQFP44: 64 | TQFP52: 72<br>TQFP64: 80 |
| **Quad Flat Non Leaded (Open Cavity QFN)** | Plastic open cavity | Thermal performance, low inductance, high frequency.<br>Theses packages need thinned dies to 250µm. | QFN12: 49<br>QFN16: 50<br>QFN20: 54<br>QFN24: 62<br>QFN28: 61<br>QFN32: 73<br>QFN36: 75<br>QFN40: 76 | QFN44: 78<br>QFN48: 80<br>QFN52: 83<br>QFN56: 86<br>QFN64: 98<br>QFN80: 107<br>QFN88: 118<br>QFN100: 131 |
| **Plastic Open Cavity Packages** | Plastic | Allows a smooth transfer between ceramic and plastic pakage (QFN, QFP, PLCC, PGA, BGA).<br>STEP 1 Dummy Package; STEP 2 "Open Cavity"; STEP 3 Wire Bonding; STEP 4 Remolding or Lid & Marking (YOUR LOGO cmp A12345) | Upon request | |
| **Optical resin [1]<br>Chip On Board (COB) [2]<br>Thermal solutions [3]<br>Metallic & Hermetic package [4]** | | [1] Transparent, clear glob top and optical adhesive.<br>[2] Direct bonding of dies on organic substractes.<br>[3] Thermal solutions: QFN, SFP, TQFP could be asked with Exposed Pad as an enbedded heat sink.<br>[4] For some applications (MEMS), it is possible to ask for hermetic sealing of ceramic packages. | Upon request | |
| **Wafer level thinning** | | ams 0.35µm (8"): standard thinning to 530µm.<br>ams 0.35µm (8"): thinning to 250µm on request STMicroelectronics 130nm (8"): standard thinning to 375µm. | Free of charge | |
| **Die level thinning** | | Down to 150µm (absolute limit 100 µm) | Area<1mm²: 10€/die<br>1mm²<Area<5mm²: 13€/die<br>5mm²<Area<10mm²: 16€/die<br>10mm²<Area<15mm²: 20€/die<br>15mm²< Area contact CMP | |
| **DRIE dicing** | Option of thinning to 50µm | Clean borders of the chips, a better precision than conventional dicing | Upon request | |



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