BCD8sP Technology Overview

Sense & Power and Automotive Technology R&D
Smart Power Technology

January 2017
What is BCD?

A concept invented by ST in the mid-80s [1][2][3] widely used today in the industry.


Analog + Digital + Power & HV on one chip

- **High Voltage or Power** section (DMOS) to drive external loads
- **Analog** blocks to interface the “external world” to the digital systems
- **Digital** core (CMOS) for signal processing
# BCD Technology Segmentation

<table>
<thead>
<tr>
<th>SEGMENT</th>
<th>TECHNOLOGY PLATFORM</th>
<th>APPLICATION FIELDS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>High Voltage BCD</strong></td>
<td></td>
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</tr>
<tr>
<td>0.32µm</td>
<td>BCD6s Offline 3.3V / 5V CMOS – 25V/800V</td>
<td>Lighting, Motors, Electrical Car</td>
</tr>
<tr>
<td></td>
<td>BCD6s HV Transformer 3.3V CMOS - Galvanic Isolation 4-6KV</td>
<td></td>
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<tr>
<td></td>
<td>SOI-BCD6s 3.3V CMOS - 20V/50V/100V/190V</td>
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</tr>
<tr>
<td></td>
<td>SOI-BCD8s 1.8V CMOS - 70V/100V/140V/200V</td>
<td>Full digital amplifier, Echography, AMOLED, Pico-projector</td>
</tr>
<tr>
<td><strong>SOI BCD</strong></td>
<td></td>
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</tr>
<tr>
<td>0.16µm</td>
<td>BCD8As 3.3V CMOS - 8V/18V/40V</td>
<td></td>
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<tr>
<td></td>
<td>BCD8sP 1.8V CMOS - 10V/18V/27V/42V/60V</td>
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<tr>
<td></td>
<td>BCD8sAUTO 3.3V CMOS - 20V/40V/65V/100V</td>
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<tr>
<td></td>
<td>BCD9s 1.8V CMOS - 10V/40V/60V</td>
<td>HDD, Airbag, Audio amplifier, Power Line modems</td>
</tr>
<tr>
<td></td>
<td>BCD9sL 3.3V CMOS - 20V/40V/65V/100V</td>
<td></td>
</tr>
<tr>
<td>0.11µm</td>
<td>BCD10 1.2V CMOS - 8V to 65V</td>
<td>Power Supply, Automotive, Power Management for Mobile</td>
</tr>
<tr>
<td><strong>Advanced BCD</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>90nm</td>
<td>HVG8 1.8V/22V/32V CMOS</td>
<td>Bio Medical, Advanced Analog</td>
</tr>
<tr>
<td></td>
<td>HVG8A 16V CMOS</td>
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</table>
BCD Evolution in the “More than Moore” arena

Driven more by Process Customization for Application Requirements than by Reduction of Lithography Node

Trend towards Advanced Technology Nodes compatible with availability of Depreciated Advanced Manufacturing Plants

Long Lifetime of Products and Process Generations

Always present demand for Cost Reduction
BCD in ST – Overview

- Solid know-how developed over three decades
  - Processes from 4.0 μm to 0.11 μm developed and produced

- Unique voltage range offering
  - Large voltage range spanning multiple application fields

- Advanced process nodes differentiated by application
  - Offers best in class HV devices with large CMOS integration capability

- Process customization by application
  - Strong synergy between technology, design and application

30 Years
5 V to 800 V
0.16 μm
0.11 μm
BCD8sP Overview

BCD8sP is a 0.16µm Technology Platform dedicated to Smart Power applications with the following main features:

- Baseline 1.8V CMOS for High Density Logic cores
- Best-in-class Power devices: 10V - 18V - 27V - 42V – 60V(*)
- Dual gate oxide process: 1.8V CMOS, 5V CMOS & Power Devices
- Optional DTI option for lateral isolation
- 4 Metal Levels with Thick Power metal
- Available memory: OTP, FTP (EEPROM)

Application examples:

- Hard Disk Drivers Power Combo
- Motor Drivers
- Printer
- DC-DC converter
- Power Management

(*) 60V available with DTI option only
## BCD8sP Device Portfolio

### Low Voltage
- 1.8V CMOS
- 5V CMOS

### High Voltage
- 10V/18V/27V/42V Power NMOS Isolated Drain
- 42V Power NMOS HS
- 15V/27V/32V/48V/60V nDrift MOS
- 15V/27V/32V/48V/60V pDrift MOS

### Bipolars
- 5V NPN
- 5V PNP HP (Isolated Vertical)
- 18V PNP (Isolated Vertical)

### Diodes
- 5V Zener, 5V Isolated Zener
- p+/Nwell, p+/HVnwell
- n+/Pwell, n+/Hvpwell

### Capacitors
- 1.8V/5V poly capacitors
- 12V poly-poly capacitor
- MOM

### Resistors
- Poly resistors (4 types), including HIPO resistor
- Diffused resistor

### ESD & IPs
- 1.8V/5V/8V/18V/42V/60V ESD protection
- OTP & NVM libraries
BCD8sP Main Features

- 1.8V CMOS with HD Digital Library (90 kGates/mm²)
- 5V CMOS and wide passive components offer for Analog design
- 4 Metal level BEOL with following options for Top Metal:
  - 3µm Thick Aluminum
  - 10µm Thick Copper (Re-Distribution Layer)
- **Best-in-class** Power devices with specification matching real application needs

<table>
<thead>
<tr>
<th>Nch MOS</th>
<th>POWER SPEC (full T range: -40 °C ÷ 125 °C)</th>
<th>POWER PERFORMANCE (T = 25 °C)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Max Operating Voltage (MOV)</td>
<td>Absolute Max Rating (AMR)</td>
</tr>
<tr>
<td></td>
<td>10 V</td>
<td>12 V</td>
</tr>
<tr>
<td></td>
<td>18 V</td>
<td>25 V</td>
</tr>
<tr>
<td></td>
<td>27 V</td>
<td>32 V</td>
</tr>
<tr>
<td></td>
<td>42 V</td>
<td>46 V</td>
</tr>
<tr>
<td></td>
<td>60 V</td>
<td>65 V</td>
</tr>
</tbody>
</table>

- Typical product masks count (based on option): **28 to 33**
Design Platform: Design Kit, supported tools & Libraries
## Design Platform – Basic Tools Supported in PDK

<table>
<thead>
<tr>
<th>Front-end/Schematic capture</th>
<th>EDA tools</th>
<th>EDA Vendors</th>
<th>Tool version (or newest)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schematic Capture (Composer)</td>
<td>IC</td>
<td>Cadence</td>
<td>IC6.1.6.500.3</td>
</tr>
<tr>
<td>Design environment</td>
<td>ArtistKit</td>
<td>ST</td>
<td>5.9</td>
</tr>
<tr>
<td></td>
<td>Spectre</td>
<td>Cadence</td>
<td>12.11.164</td>
</tr>
<tr>
<td></td>
<td>Eldo</td>
<td>Mentor</td>
<td>13.1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Layout Entry &amp; Finishing</th>
<th>EDA tools</th>
<th>EDA Vendors</th>
<th>Tool version (or newest)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layout Placement</td>
<td>Virtuoso Layout Editor</td>
<td>Cadence</td>
<td>IC6.1.6.500.3</td>
</tr>
<tr>
<td>Layout Verification</td>
<td>Calibre ViPVS</td>
<td>Mentor Cadence</td>
<td>2013.1_14.11 13.10.286</td>
</tr>
<tr>
<td>Parasitic Extraction: interconnect RC</td>
<td>Star-RCXT</td>
<td>Synopsys</td>
<td>i-2013.12-1</td>
</tr>
</tbody>
</table>

**Metal options available:** 4M Al – 4M Cu RDL
Design Platform – Full List of supported Tools

**Cadence**
- IC 6.1.6.500.3 (Virtuoso Framework)
- Spectre 12.11.164 (Analog Simulator)
- ViPVS 13.10.286 (Layout Verification)
- mmsim 12.11.164 (Analog simulator environment)
- incisiv 13.10.001 (Simulation Verification Environment)
- Conformal 12.10.300 (Formal Verification)
- Rc 12.20.000 (Synthesis)
- edi 13.2usr3 (P&R)
- IC 6.1.6.500.3 (VSR AnalogRouter)

**Synopsys**
- Star-RCXT i-2013.12-1 (Parasitic Extraction)
- hsimplus i-2013.12 (Tx Level Simulator)
- mvtools g-2012.09-4 (Static checker)
- vcsmx h-2013.06-sp1 (Digitla simulator)
- xa i-2013.12 (Tx Level Simulator)
- Primetime h-2013.06-sp2 (STA)
- PrimeRail i2011.12 (Digital IRDrop)
- Synthesis h-2013.03-sp3
- Tetramax h-2013.03-sp3 (ATPG)
- Formality h-2013.03-sp3 (Formal Check)
- Galaxy-ca h-2013.06-sp2 (Constraint Analyzer)
- Iccompiler g-2012.06-sp5 (P&R)
- Hercules y-2006.12-sp2-6 (Cheker for Prme Rail)

**Mentor**
- Eldo/Eldo Premier 13.1 (transistor level)
- Questa-ADMS 13.1 (mixed-signal cosimulation)
- Calibre 2013.1_14.11 (Layout Verification)
- QuestaSim 10.2.b (digital simulation)
### Design Platform – Digital Libraries/IPS

<table>
<thead>
<tr>
<th>Digital Library</th>
<th>BCD8000HDS – (1.8V CMOS)</th>
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<tbody>
<tr>
<td>SP Analog IPs</td>
<td>Macrocells_ESD</td>
</tr>
<tr>
<td>Memory Compilers</td>
<td>Single port RAM (2 compilers)</td>
</tr>
<tr>
<td></td>
<td>OTP (1 to 16) x (8/16) bits</td>
</tr>
<tr>
<td></td>
<td>Cut service available on request</td>
</tr>
<tr>
<td>IO’s Libraries</td>
<td>3V3FT 4MAI (3V capable 5V tolerant GPIO)</td>
</tr>
<tr>
<td></td>
<td>5V0 4MAI (5V capable GPIO)</td>
</tr>
<tr>
<td>Power Devices Library</td>
<td>«Ready-to-use» Power Devices layout</td>
</tr>
<tr>
<td></td>
<td>Cut service available on request</td>
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</tbody>
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Thank You