On behalf of the Program and Executive Committees, it is my pleasure to invite you to IEEE’s 67th Electronic Components and Technology Conference (ECTC), which will be held at the Walt Disney World Swan & Dolphin Resort, Lake Buena Vista, Florida, from May 30 to June 2, 2017. All ECTC meetings will be taking place in the Walt Disney World Dolphin Resort building.

This premier international annual conference, sponsored by the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society, brings together key stakeholders of the global microelectronics packaging industry, such as semiconductor companies, foundry and OSAT service providers, equipment manufacturers, material suppliers, research institutions and universities, all under one roof. More than 1,400 people attended the 66th ECTC in Las Vegas, Nevada, in May 2016.

At the 67th ECTC, more than 360 technical papers are scheduled to be presented in 36 oral sessions and five interactive presentation sessions, including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as flip chip packaging, 3D/TSV technologies, wafer level packaging, design for RF performance and signal/power integrity, thermal and mechanical modeling, optoelectronics packaging, materials and reliability.

Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Authors from 22 countries are expected to present their work at the 67th ECTC, covering ongoing technological challenges with established disciplines or emerging topics of interest for our industry, such as additive manufacturing, heterogeneous integration, and flexible and wearable electronics.

ECTC will also feature panel and special sessions with industry experts covering a number of important and emerging topic areas. On Tuesday, May 30 at 10 a.m., Vikas Gupta and Pradeep Lall will chair a session on “Material and Package Reliability Needs/Challenges for Harsh Environments.” That same day at 2 p.m., Bing Dang will chair a panel session on “Flexible Hybrid Electronics – Electronics Outside the Box,” where a panel of experts will discuss how innovation in device integration and packaging will bring together thinned silicon die with printed components to deliver electronics that conform to the shape of the human body and vehicles. Tuesday evening will also include the ECTC Panel Session at 7:30 p.m. on “Panel Fan-Out Manufacturing: Why, When, and How?” chaired by CPMT President Jean Trewhella and Young Gon Kim.

Continuing to build on the success of the first-ever CPMT Women’s Panel and Reception held at the 65th ECTC, this year’s conference will also feature a panel discussion chaired by Kitty Pearsall on Wednesday, May 31, at 6:30 p.m. on “Emotional Intelligence (EI) – Link to Successful Leadership,” with participation from distinguished women leaders and technologists in our industry. All conference attendees are invited. Also on Wednesday at 7:30 p.m., Luke England will chair the ECTC Plenary Session titled “Packaging for Autonomous Vehicle Electronics,” featuring key technologists sharing their views on the evolutionary requirements for packaging and reliability challenges to support widespread implementation of driver-less vehicles on the road. On Thursday, June 1 at 8 p.m., the CPMT Seminar titled “3D Printing Tools, Technologies and Applications,” will be moderated by Venkatesh Sundaram and Yasumitsu Orii from the High-Density Substrates & Boards Technical Committee of the CPMT Society.

Supplementing the technical program, ECTC also offers several Professional Development Courses (PDCs) and Technology Corner exhibits. Co-located with the IEEE ITherm Conference this year, the 67th ECTC will offer 18 PDCs, organized by the PDC Committee chaired by Kitty Pearsall. The PDCs will take place on Tuesday, May 30th and are taught by distinguished experts in their respective fields. The Technology Corner will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging and services fields. More than 100 Technology Corner exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. I invite you to make your plans now to join us for the 67th ECTC and be a part of all the exciting technical and professional opportunities. I also take this opportunity to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 67th ECTC a success. I look forward to meeting you in Lake Buena Vista, Florida, from May 30 to June 2, 2017.

Mark D. Poliks
67th ECTC Program Chair
Binghamton University
Phone: +1-607-777-5361
Email: mpoliks@binghamton.edu

**Index**

ECTC Registration ................................................. 3, 31, 32
General Information .................................................. 3
Hotel Information ..................................................... 3, 31
2017 ECTC Special Session ........................................ 4
2017 Technical Subcommittee Special Session ............. 4
2017 ECTC Panel Session ......................................... 4
2017 ECTC Plenary Session ....................................... 4
2017 CPMT Seminar .............................................. 5
ECTC Luncheon Keynote Speaker ............................. 5
Luncheons and Receptions ........................................ 5
2017 CPMT Women’s Panel and Reception .................. 5
Executive and Program Committees ......................... 6-7
Professional Development Courses .......................... 9-14
Area Attractions .................................................... 14
Program Sessions ................................................... 15-30
2017 Technology Corner Exhibits .............................. 31
Conference Overview ............................................. 35
**67th ECTC ADVANCE REGISTRATION**

**Advance Registration**

Online registration is available at www.ectc.net. For more information on registration rates, terms, and conditions see page 32.

Register early ... save US$100 or more!

All applications received after May 4, 2017 will be considered Door Registrations. Those who register in advance can pick up their registration packets at the ECTC Registration Desk in the Dolphin Convention Center on the Lobby Level in front of Australia 3. Please note that the Swan and Dolphin are two separate buildings, and all ECTC meetings will be taking place in the Walt Disney World Dolphin Resort.

**On-Site Registration Schedule**

<table>
<thead>
<tr>
<th>Date</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Monday, May 29, 2017</td>
<td>3:00 p.m. to 5:00 p.m.</td>
</tr>
<tr>
<td>Tuesday, May 30, 2017</td>
<td>6:45 a.m. to 5:00 p.m.*</td>
</tr>
<tr>
<td>Wednesday, May 31, 2017</td>
<td>6:45 a.m. to 4:00 p.m.</td>
</tr>
<tr>
<td>Thursday, June 1, 2017</td>
<td>7:30 a.m. to 4:00 p.m.</td>
</tr>
<tr>
<td>Friday, June 2, 2017</td>
<td>7:30 a.m. to 12:00 noon</td>
</tr>
</tbody>
</table>

*6:45 a.m. to 800 a.m. (Morning PDCs & morning ECTC Special Session Only)

**General Information**

Conference organizers reserve the right to cancel or change the program without prior notice. Please note that the Walt Disney World Swan and Dolphin Resort are two separate buildings, and all ECTC meetings will be taking place in the Walt Disney World Dolphin Resort. While booking your hotel reservation please make sure to specify that you require to be placed in the Walt Disney World DOLPHIN Resort. While these two buildings are located adjacent to each other and share many of the same social / resort function areas, we want to ensure you have a most convenient experience while at ECTC 2017.

**ITherm 2017**

This year ITherm is co-located with ECTC! All ITherm sessions will take place in the SWAN building of the Walt Disney World Swan and Dolphin Resort. All ECTC sessions, and the co-location of exhibits, will take place in the DOLPHIN building.

**Loss Due to Theft**

Conference management is not responsible for loss or theft of personal belongings. Security for each individual’s belongings is the individual’s responsibility.

**ECTC Sponsors**

With 66 years of history and experience behind us, ECTC is recognized as the premier semiconductor packaging conference and offers an unparalleled opportunity to build relationships with more than 1,000 individuals and organizations committed to driving innovation in semiconductor packaging.

We have a limited number of sponsorship opportunities in a variety of packages to help get your message out to attendees. These include Gala, Program, and several other sponsorship options that can be customized to your company’s interest. If you would like to enhance your presence at ECTC and increase your impact with a sponsorship, please take a look at our sponsorship brochure on the website www.ectc.net under “Sponsors.”

To sign up for sponsorship or to get more details, please contact Wolfgang Sauter at wolfgang.sauter@globalfoundries.com or +1-802-922-3083.

**Hotel Accommodations**

Rooms for ECTC attendees have been reserved at the Walt Disney World Dolphin, of the Walt Disney World Swan and Dolphin Resort. The special conference rate is:

**$189.00 / Run of the House**

Please note these rooms are on a first come, first served basis. If this specific category is no longer available, attendees will be offered the next best available accommodation. These prices include single or double occupancy in one room. Please note that rooms offering two beds are limited and subject to availability and should be requested at the time of reservations.

Room reservations must be made directly with the hotel by **Friday, May 5, 2017**, at 5pm ET to ensure our preferred conference rate. All reservations made after the cutoff date of Friday, May 5, 2017, at 5pm ET will be accepted on a space and rate available basis. **If you need to cancel a reservation, please do so at least 5 DAYS prior to arrival for a full refund.** Each attendee is subject to the terms and polices set by each hotel.

**Note about Hotel Rooms**

Attendees should note that only reputable sites should be used to book a hotel room for the 2017 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2017 from 3rd party companies. These emails and sites are not to be trusted. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. ECTC’s only authorized site for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that you have personally used in the past to book travel. Please be advised, there are scam artists out there, and if it’s too good to be true, it likely is. Should you have any questions about booking a hotel room please contact ECTC staff at: lrenzi@renziandco.com

**Transportation Services**

Enjoy a complimentary water taxi from the resorts’ dock, running to and from Epcot® and Disney’s Hollywood Studios™.

Complimentary shuttle buses also transport guests from the hotel entrance to Magic Kingdom® Park, Disney’s Animal Kingdom® Theme Park, Downtown Disney® area, and Disney’s Blizzard Beach Water Park and Disney’s Typhoon Lagoon Water Park.

There is, unfortunately, no courtesy transportation between the hotel and the airport.
Flexible Hybrid Electronics – Electronics Outside the Box

A rapidly maturing set of materials and manufacturing processes offers the opportunity for a new generation of electronics that leaves behind today’s bulky, rigid, and heavy packaging. Through innovations in device integration and packaging, Flexible Hybrid Electronics (FHE) will bring together thinned or unpackaged silicon die with printed components to deliver electronics that conform to the shape of the human body and vehicles. This panel discussion will address both potential applications in the neighborhood of one to two years. Electronics manufactured for extreme environment applications often have longer design life from 25-30 years, in addition to expectation of sustained operation at environment extremes.

In this special session, perspectives will be shared by companies from each of the application spaces, in addition to the companies that make materials and components for usage in each of the application spaces. The focus will include the application needs and the material and packaging solution-paths to meeting the survivability and performance requirements.

1. Erick W. Seltmann, Boeing
2. Przemyslaw Jakub Gronada, Bosch
3. Steve Dunford, Schlumberger
4. Anton Z. Miric, Heraeus Deutschland GmbH & Co. KG
5. Emad A. Andarawis, General Electric
6. Varughese Mathew, NXP Semiconductors

Fan-out packaging has proven to be a versatile solution – cost-effective for low-end applications and high-performance for leading-edge products. They provide flexibility with design rules, number of RDL layers, component sourcing, and even passive component embedding. Hence, fan-out is now taking off and is projected to be the fastest growing packaging approach. It can be done in either a wafer or panel format. Wafer format fan-out packaging processing shares many features with conventional WLCSP. Thus, this infrastructure similarity enabled adoption of this technology with less market resistance than is typically seen with new manufacturing processes.

However, panel format processing for fan-out packaging has been evolving with a different path. Large panels can process four wafers or more at one time, which provides significant cost benefits. Unfortunately, panel fan-out introduces multiple challenges, including significant capital investment, unique process issues, and industry standardization. We believe that the significant cost benefits provide motivation to migrate to panel format fan-out processing. The remaining key question on panel fan-out might be ‘when’, which could be determined by the return on investment (ROI) driven by market demand.

This panel session aims to look at various views from fan-out packaging experts: two from wafer format fan-out manufacturers, two doing extensive development on panel fan-out, and one focused on cost-effective solution search for product applications. We expect the discussion to help those who want to develop accurate fan-out packaging technology roadmaps.

1. Douglas Yu, TSMC
2. Tim Olson, DECA
3. Steffen Kroehnert, NANIUM
4. Rolf Aschenbrenner, IZM Fraunhofer
5. Steve Bezuk, Qualcomm Technologies, Inc.

These sessions are open to all conference attendees.
our Gala Reception sponsors. All badged attendees and their guests are invited to attend a reception hosted by
meet otherwise!
Enjoy good food and network with industry leaders and achievers. Don’t miss
have the opportunity to talk with industry professionals about what helped
industry and how you could use your technical skills and innovative talent? If
Students, have you ever wondered what career opportunities exist in the
become a mainstream technology and overcome for 3D printing to become a mainstream
together with local manufacturing and end users. The trend is expected to continue in the future. It is
complete device without any assembly processes. The system is operated according to 3D
customized wearable devices or IoT sensor modules. These systems can form electronic devices such as
functions with so-called “functional 3D printing systems.” These systems can form electronic devices such as
technologies as flexible electronics.
By Invitation Only

ECTC Luncheon Keynote Speaker

Advanced Packaging Opportunities and Challenges
Wednesday, May 31, 2017, 12:00 Noon
Presenter: Babak Sabi,
Corporate Vice President and Director of Assembly and Test Technology Development, Intel Corporation

Industry reliance on advanced packaging has been accelerating over the last few years. This trend is expected to continue in the future. Heterogeneous integration of multiple chips in a package supports Moore’s Law scaling and is driving many challenges in package interconnect scaling, design environment, optical integration, electrical/thermal performance, and test. Babak Sabi, Corporate Vice President and Director of Assembly and Test Technology Development at Intel Corporation, will address future challenges and opportunities for advanced multi-chip packaging.
Since 2009, Babak has been responsible for Intel’s packaging, assembly process, packaging materials, enabling technology, and test technology development. Prior to leading Assembly and Test Technology Development, Babak led the Corporate Quality Network within Intel’s Technology and Manufacturing Group from 2002 to 2009. He also led a company-wide network of quality and reliability organizations responsible for product reliability, customer satisfaction, and quality business practices. Previously, Babak managed technology development quality and reliability, and was responsible for silicon technology certification, assembly, test, and board processes. Babak joined Intel in 1984, the same year he received his Ph.D. in solid state electronics from The Ohio State University.

ECTC Luncheon

Tuesday, May 30, 2017 – 6:00 p.m. – 7:00 p.m.
(by invitation only)

General Chair’s Speakers Reception
Tuesday, May 30, 2017 – 6:00 p.m. – 7:00 p.m.

ECTC Student Reception
Tuesday, May 30, 2017 – 5:00 p.m. – 6:00 p.m.

Students, have you ever wondered what career opportunities exist in the industry and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk with industry professionals about what helped them be successful in their first job search and reach their current positions. Enjoy good food and network with industry leaders and achievers. Don’t miss the opportunity to interact with people that you might not have the chance to meet otherwise!

Exhibitor Reception
Wednesday, May 31, 2017 – 5:30 p.m. – 6:30 p.m.

67th ECTC Gala Reception
Thursday, June 1, 2017 – 6:30 p.m.

All badged attendees and their guests are invited to attend a reception hosted by our Gala Reception sponsors.

2017 CPMT Women’s Panel and Reception

Emotional Intelligence (EI) – Link to Successful Leadership
Wednesday, May 31, 2017, 6:30 p.m. – 7:30 p.m.
Chair: Kitty Pearshall - Boss Precision, Inc.

CPMT Society President Jean Trewhella and 67th ECTC Past General Chair Beth Keser cordially invite all ECTC attendees to attend our third Women’s Panel and Reception sponsored by CPMT. The three panelists will speak on their experiences and achievements in the microelectronics industry and provide insights into how Emotional Intelligence enabled them to be successful leaders. A Q&A session and reception for panelists and attendees will follow.
1. Joanne Martin, JLM Consulting, LLC and former Vice President, IBM Corporation
2. Rosalio Becco, Global Director New Business Development, The Dow Chemical Company
3. Tanja Braun, Deputy Group Manager, Fraunhofer Institute for Reliability and Microintegration IZM

LUNCHEONS

Tuesday PDC Luncheon
All individuals attending a PDC course are invited to join us for lunch on Tuesday, May 30. Proctors and instructors are welcome, too!

Wednesday Conference Luncheon
Please be sure not to miss our Wednesday luncheon with guest speaker Babak Sabi, Corporate Vice President and Director of Assembly and Test Technology Development, Intel Corporation. All conference attendees are welcome!

Thursday CPMT Luncheon
Our sponsor, the IEEE Components, Packaging and Manufacturing Technology Society, will be sponsoring lunch on Thursday for all conference attendees!

Friday Program Chair Luncheon
Please attend Friday’s lunch hosted by the 67th ECTC Program Chair. We will honor conference paper award recipients and raffle off a vast array of prizes including a hotel stay, free conference registrations, and many other attractive items!

2017 CPMT Seminar

3D Printing Tools, Technologies and Applications
Thursday, June 1, 2017, 8:00 p.m. – 9:30 p.m.
Chairs: Venky Sundaram - Georgia Institute of Technology and Yasumitsu Orii - Nagase, Japan

Due to the trend towards a globalized, technical and connected society, there is a rising demand for a new breed of technologies enabling low-priced, flexible and new-concept products. Conventional technologies (including silicon based microelectronics) have reached their limits due to their high fabrication costs and environmental issues. Armed with new printing technologies (including screen, gravure, reverse gravure, flexo, offset, ink jet, etc.) and innovative materials, printed electronics has recently emerged as a promising environmentally friendly alternative route to produce electronic/display/energy products at a low cost and with new possibilities of such creative technologies as flexible electronics.
3D printing systems (forming 3D structure) have already become an indispensable tool in a wide variety of industrial fields. 3D printing has now started to impact electronic functions with so-called “functional 3D printing systems.” These systems can form electronic devices such as customized wearable devices or IoT sensor modules on-demand. The system is operated according to 3D CAD data, including electronic circuits and insulation layer position and electronic parts position and then produces a complete device without any assembly processes.
However, there are still a lot of technical barriers to overcome for 3D printing to become a mainstream process for manufacturing devices, packages and systems. This seminar will highlight important recent developments in 3D printing tools, technologies and applications and conclude with a brief panel discussion.
1. Manos Tentzeris, Georgia Institute of Technology
2. Humar Mandalwa, Zekun SOZO Center
3. Simon Fried, Nano Dimension Ltd.
4. Takeshi Sato, Fuj Machine Mfg., Co., Ltd.
Innovative IC, System-in-Package, and MEMS packaging portfolio for today’s miniaturization, mobility, and IoT needs.

Wire Bond  Flip Chip  WLP  2.5D & 3D  Fanout  SiP

Packet it.
@asegroup_global  aseglobal.com

Advantages include:
• Low-temperature bonding 25°C to ≤ 100°C
• Increased throughput
• High-temperature survivability ≤ 350°C
• Increased adhesion at all interfaces
• Post-bond total thickness variation ≤ 5% of the nominal bond-line thickness
• Reduced baking & cleaning times
• Compatible with mechanical or laser debonding

Looking to improve your Polymer Cure?

The answer is YES-VertaCure
Automated High Temperature Vacuum Cure Oven

Transforming atomic-scale engineering with market-leading deposition, etch, and clean technologies for front-end wafer processing and advanced packaging applications

Learn how our innovative solutions can help you achieve success on the wafer

www.lamresearch.com

Look to improve your Polymer Cure?

The answer is YES-VertaCure
Automated High Temperature Vacuum Cure Oven

Increase:
ROI
Product Yield

Decrease:
Polymer bake time
Outgassing at metallization, from polymer & molding compound

www.yieldengineering.com
1.888.YES.3637
1. ACHIEVING HIGH RELIABILITY OF LEAD-FREE SOLDER JOINTS – MATERIALS CONSIDERATIONS

Course Leader: Ning-Cheng Lee – Indium Corporation

Course Objectives:
This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMC) under a variety of material combinations and aging conditions and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, and fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in detail. Novel alloys with reduced fragility will be presented. Electromigration, corrosion, and tin whisker growth will also be discussed. Furthermore, the reliability of through-hole solder joint will be reviewed, and recommendations will be provided, particularly for thick boards. The emphasis of this course is placed on the understanding of how the various factors contribute to the failure modes, and how to select proper solder alloys and surface finishes for achieving high reliability. Also presented are the desirable future alloys and fluxes in order to meet the challenge of miniaturization.

Course Outline:
1. Implementation Status
2. Prevailing Materials: Alloys and Finishes
3. Surface Finishes Issues: ENIG, Immersion Ag, and Immersion Sn
4. Mechanical Properties: Shear, Pull, and Creep
5. Intermetallic Compounds: Effect of Cu, Ni, Other Additives, and Heat History
6. Failure Modes: Grain Deterioration, Orientation, Mixed Alloys, and Interfacial Voiding
7. Thermal Cycle Reliability: Effect of Cycling Condition, Surface Finishes, and Rafflow Temperature
8. Reliability of Through-Hole Joints: Large and Thick Boards, Partially Filled Through-hole
9. Fragility: Effect of Surface Finishes, Alloys, Rafflow, Strain Rate, Aging, Cycling, and IMC
10. Electromigration: Effect of Current Density, Back Stress, and Cu UBM Thickness

2. WAFER LEVEL-CHIP SCALE PACKAGING

Course Leader: Luu Nguyen – Texas Instruments, Inc.

Course Objectives:
This course will provide an overview of the Wafer Level-Chip Scale Packaging (WL CSP) technology. The market drivers, end applications, benefits, and challenges facing industry-wide adoption will be discussed. Typical WL CSP configurations (bump-on-pad, bump-on-polymer, fan-in, and fan-out) will be discussed in terms of their construction, manufacturing processes, materials and equipment, and electrical and thermal performance, together with package and board level reliability. Extensions to higher pin count packages and other areas such as RF sensors and MEMS will be reviewed.

Future trends covered will include enhanced lead-free solder balls, large die size, wafer level underfill, thin and ultra-thin WL CSP, RDL (Redistribution Layer), stacked WL CSP, MCM in “reconstituted wafers,” embedded components, and applications to large format (panel) processing. Since the technology marks the convergence of fab, assembly, and test, discussion will address questions on the industrial supply chain such as: Does it fit best with front-end or back-end processing? Are the current standards for design rules, outline, reliability, and equipment applicable? Will it be applicable and cost-effective for memory and other complex devices such as ASICs and microprocessors?

Course Outline:
1. Market Drivers for WL CSPs: Handsets, Medical, Automotive, Space, Imaging Sensors, MEMS, HBI LEDs
2. Key WL CSP Technologies
3. Equipment and Materials Tool Box
4. Infrastructure Service Providers
5. PCB Pitch Reduction
6. Cost, Benefits, and Drawbacks of WLPs
7. Reliability: Thermal Cycling, Drop, Flex Testing, Electromigration
8. Fan-Out WLP
9. Supply Chain
10. Embedded Die
11. Chip First vs. Chip Last
12. Single Die Embedding vs. SIP Module
13. Challenges and Evolution to Large Format Processing

Who Should Attend:
The course will be useful to the following groups of engineers: Newcomers to the field who would like to obtain a general overview of WL CSP; R&D practitioners who would like to learn new methods for solving CSP problems; and those considering WL CSP as a potential alternative for their packaging solutions.

3. LED PACKAGING, SYSTEM, AND RELIABILITY CONSIDERATIONS

Course Leader: Xuejun Fan – Lamar University

Course Objectives:
The light emitting diode (LED) has now emerged as a promising technology to replace conventional lighting, such as incandescent bulbs and compact fluorescent lamps, due to its superior energy efficiency, environmental friendliness, and particularly long lifetime (in the range of 25,000 – 100,000 hours). This course will present a comprehensive overview of recent advances in LED packaging, system integration, and reliability issues. Unlike traditional IC failure that is mainly characterized by catastrophic mode, LEDs’ performance is characterized by a dual-degradation mode: light output (lumen maintenance) degradation and color shift. Packaging structure, system integration, and materials play a very important role in LED efficacy and reliability. This course will cover the topics below:

Course Outline:
1. LED Introduction
2. LED Basics
3. LED Packaging and System Integration
4. Basics of LEDs’ Photometry and Colorimetry
   - LED Packaging Evolution
   - LED Packaging Materials: Chip, Phosphor, Silicone, Reflectors, Substrate, and System Integration
5. LED Packaging Materials and Degradation
6. LED Failure Mechanisms
7. LED Testing Standards and Specifications
8. Accelerated Testing and Lifetime Prediction
9. LED Driver and LED Driver Reliability
10. Thermal Management
11. Multi-Physics Modeling
12. Physics of Failure (PoF) Based Health Monitoring
13. System Reliability and Prediction
14. Conclusions

Who Should Attend:
The course is designed for staff members, technical managers, LED system reliability, design and manufacturing personnel, reliability engineers, and students who are interested in LED packaging, material selection, and LED reliability. The course does not assume prior knowledge in LED areas.

4. FUTURE OF DEVICE AND SYSTEMS PACKAGING: STRATEGIC TECHNOLOGIES, MFG. INFRASTRUCTURE, AND APPLICATIONS

Course Leader: Rao Tummala – Georgia Institute of Technology

Course Objectives:
The semiconductor and systems landscape is changing dramatically. ICs are becoming commodities providing much lower profit margins than ever before, leading to industry consolidation to less than ten manufacturing companies within the next decade, worldwide. In addition, the cost and complexity of
transistor scaling is growing exponentially. There is no longer a cost reduction as the next node is introduced with higher transistor density. In addition, IC performance is being greatly impacted by interconnect delay and leakage.

The driving engines for electronic systems are also changing dramatically to smart, wearable, wireless healthcare, wireless networks and new era of self-driving and electric cars, requiring an entirely different vision and strategy than transistor scaling alone that has been and continues to be practiced the last 60 years. These systems are small to ultra-small systems, yet must perform dozens of functions that include high-speed digital, high-efficiency power, 5G and millimeter wave, MEMS, and sensors. The new era of automotive electronics, in addition, requires a variety of sensing technologies for self-driving cars such as camera, LiDAR and radar, and ultra-high power for electric cars. All these emerging or next-generation computing, communications, consumer and automotive systems pose device, packaging and integration barriers.

They require a new role for packaging. Future packaging must address these devices and systems’ challenges by enabling better and cheaper devices and highly-integrated and ultra-miniaturized systems. The advances need to be more than Moore’s (MTM) Law with on-chip transistor integration with 2D and 2.5D MCM, 3D stacked ICs with TSV and SIP. They require a new paradigm in systems packaging, referred to as “System Moore’s” Law (SM) for complete systems. Such a concept requires new system package architecture beyond SIP, 2.5D and 3D with TSV.

The course will review the current approach to devices, device packaging and system packaging. These include traditional single and multi-chip packaging as well as the recent focus in embedded and fan-out packaging. This course describes IC and system packaging challenges and potential solutions that lie ahead in strategic technologies, manufacturing infrastructures and applications.

Course Outline:

1. Emerging Electronic Systems
2. Current Approach to Devices and Device Packaging
3. Strategic Packaging Technologies to Enable Future Devices
   - Integration of Homogeneous and Heterogeneous Devices in 2D, 2.5D, and 3D Multi-Chip Packaging which Requires I/O Scaling Similar to BEOL
4. Strategic Systems Packaging Technologies to Enable Future Systems
   - Envisioned is a System Scaling Concept that includes Devices by Transistor Scaling but Goes Beyond to include Components and Interconnections
5. Current vs. Future Packaging Manufacturing Infrastructure
   - Current: Limited to Wafer-Based with BEOL Tools or Panel-Based Tools with Low I/O Density
   - Future: Panel-Based BEOL-Like Packaging
6. Emerging and High-Growth Applications
7. Applications of Future Packaging to Emerging Systems

Who Should Attend:
Senior marketing and R&D executives as well as senior managers who are dealing with strategic issues facing the electronics industry should attend.
processes and electrical design of glass and silicon interposers, including their RDLs. An overview of advanced packaging technologies and the role of interposers will first be given. This will be followed by a thorough discussion of silicon interposers, through-silicon via (TSV) generation process and tools, as well as glass interposers and options for through-glass vias (TGV) generation and metallization. Major challenges of RDL build-up on thin interposer substrates will be presented and advanced RDL materials and technologies to realize routing down to 3 µm in interposers will be discussed. The fundamentals of efficient electrical design of interposers and RDLs up to millimeter-wave frequencies will be given. Finally, the RF performance of transmission lines and vias in these interposers will be compared. Examples of interposers designed and fabricated at Fraunhofer IZM will also be discussed.

Course Outline:
1. Introduction to Advanced Packaging Technologies and the Role of Interposers
2. Silicon Interposers: Illustration of TSV Generation Process and Tools
3. Glass Interposers: Illustration of Technology Options for TGV Generation and Metallization
4. Presentation of Thin Substrate Handling and Temporary Bonding
5. Comparison between Glass, Silicon and Organic-Based Interposers
6. Illustration of RDL Generation and their Role in CSP and FO-WLP
7. Discussion of Major Challenges of RDL Build-Up on Thin Interposer Substrates
8. Advanced RDL Materials/Technologies to Realize Routing Down to 3 µm in Interposers
9. Electrical Design Challenges of Interposers and RDLs: Signal/Power Integrity and EMI issues
10. New Design Approach for Applications up to Millimeter-Wave Frequencies
11. Explanation of Fundamental Electrical Design Concepts: Impedance, RLCG Parasitics, S-Parameters
12. Electrical Design, Measurement and Comparison of Transmission Lines on RDLs and Interposers
13. Electrical Design, Measurement and Comparison of TSVs and TGVs
14. Examples of Interposers Designed, Fabricated and Characterized at Fraunhofer IZM

Who Should Attend:
Engineers, researchers, designers, technical managers and graduate students involved in the process of electrical design, layout, processing, fabrication and/or system-integration of interposers and electronic packages.

8. INTRODUCTION TO MECHANICS BASED QUALITY AND RELIABILITY ASSESSMENT METHODOLOGY
Course Leaders: Shubhada Sahasrabudhe and Sandeep Sane – Intel Corporation

Course Objectives:
This course presents a unique integrated methodology that combines two essential domains, engineering mechanics and reliability statistics, to perform standards-based or knowledge-based risk assessment to meet the dynamic market demand for electronic devices. To ensure that corporate Q&R goals are met, it is vital to have a comprehensive understanding of device usage and complete characterization of physics of failure. This course discusses key elements of Q&R like use conditions (UC), accelerated life tests, statistical data analysis methods, acceleration factor models, DFM risk assessment at UC, FA tools/techniques, design for reliability and experiment planning. In addition, it provides an overview of the fundamental concepts of solid mechanics such as stress-strain curves, characterization of material behavior, stress analysis methods including finite element analysis (FEA) with special application to packaging, material characterization metrologies and FEA model validation techniques. The course offers a deep dive into a few key mechanisms such as Si-package interactions, SiJ, die cracking, etc. to highlight successful application of this integrated methodology. They highlight benefits of driving proactive product risk assessment at UC and optimizing product design/process/materials for manufacturability/quality/reliability. The course will explore the application of this integrated methodology in traditional and new markets like wearables and Internet of Things. Students will perform multiple hands-on exercises throughout the duration of the course to reinforce the fundamental concepts and the value of integrated methodology.

Course Outline:
1. Packaging Technology: Trends and Challenges
2. Introduction to Quality and Reliability
3. Overview of Key Components of Reliability Statistics and Accelerated Testing
4. Hands-On Class Exercise I
5. Introduction to Solid Mechanics
6. Key Components of Solid Mechanics: Stress/Strain Curves, Failure Theories, FEA
7. Material Characterization Metrologies and Analysis Validation Techniques
9. Overlapping Areas between Reliability and Mechanics
10. Overview of the Unified Reliability Assessment Methodology Using Mechanics
11. Application of Methodology to Key Organic Package Failures
12. Hands-On Class Exercise 2
13. Summary of Key Learning Elements

Who Should Attend:
Packaging engineers involved in design, development, production, and reliability testing of semiconductor packages would benefit from the course.

9. THERMO-ELECTRIC COOLERS: CHARACTERIZATION, RELIABILITY, AND MODELING
Course Leader: Jaime Sanchez – Intel Corporation

Course Objectives:
Thermo-electric coolers are devices widely used in the semiconductor industry as the main thermal engines for thermal control during test of integrated circuit devices. They offer the ability to both heat and cool a device under test to mimic worst-case platform conditions and defect screening at different temperatures. In this short course, we will review fundamental characterization techniques of thermoelectric coolers that allow the direct measurement of relevant properties such as the effective Seebeck coefficient, electrical resistivity, and thermal impedance. A detailed numerical modeling approach will be discussed that utilizes user-defined functions in Fluent that allows a close representation of these devices matching experimental conditions. Experimentation and numerical analysis techniques will be discussed that enable the full characterization of a thermal solution based on thermo-electric coolers both in steady and transient state. A comprehensive overview of modeling and experimentation techniques will be provided that capture the dynamic behavior of a thermal solution connected to a closed loop control algorithm: the impact of various approaches of controlling the junction temperature of a device under test under different conditions, as well as the sensitivity of the dynamic response of the full system including the effect of active power management of the device under test. Finally, experimental techniques based on reliability statistics will be covered that have a direct application into predicting the life of a thermo-electric cooler under various test conditions.

Course Outline:
1. Introduction
• State-of-the-Art in Thermo-Electricity Research
• What is Thermo-Electricity
• General Industrial Applications
2. TEC Modules Governing Principles
• Single Peltier Couple to a TEC Module
• Governing Equations and Relationships
• Example of TEC Module Selection Based on a Static Cooling Application
3. TEC Module Characterization and Modeling
• Experimental Setups and Methodology
• Overview of Analytical Approaches
• Overview of Transient Characterization
4. Operation of TEC Modules in Dynamic Closed Loop Control
• Applications to Test ICs
5. Reliability of TECs
• Overview of Failure Modes
• Improvements for Test Application
6. Summary and Future Directions
7. References

Who Should Attend:
This course is intended for students and engineers in the electronics cooling industry specifically, but should be of interest for those working with thermo-electric modules in general. The class will cover experimental and numerical methods.

AFTERNOON COURSES
1:15 p.m. – 5:15 p.m.

10. FLIP CHIP TECHNOLOGIES
Course Leaders: Eric Perfecto – GLOBALFOUNDRIES and Shengmin Wen – Synaptics Inc.

Course Objectives:
This course will cover the fundamentals of flip-chip assembly process that involves wafer bumping, solder joint formation, substrate and/or redistribution selection, and underfill processes. All aspects of bumping technologies, including lead-free solder bumping and highly customized Cu Pillar technologies used in today’s flip-chip are addressed in depth, including the details and comparison of various UBM (electroplating, electroless plating and sputtering) and solder (electroplating, ball drop, IMS, and solder screening) deposition methods. Solder joint formation technologies used in single and multi-die assembly of chip scale packages, wafer-level packages, chip-on-chip, chip-on-wafer, and 2.5D/3D flip chip packages are discussed and demonstrated through
industrial’s leading application examples. The course provides a list of items to consider when choosing a particular flip-chip assembly process for a specific application such that a reliably and cost-effective solution can be planned out of various methods to bump the wafer and different substrates types (organic laminate, ceramic, and Si substrates). Chip package interaction (CP), package warpage control, and yield detractors for flip-chip assembly are discussed in detail. Advanced and current trend of flip-chip assembly processes are provided briefly. This course will cover the reliability tests commonly used to qualify the flip-chip assembled packages, the failure types and the analytical tools used to identify defect root cause. A substantial portion of this course will cover Cu Pillar flip-chip technologies. Failure modes, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, electromigration, etc. will be dispersed within the related subjects of the whole course. Students are encouraged to bring topics and technical issues from their past, present and future job function for group discussions. A 20-minute group exercise at the end of the class is planned to make sure the students can walk away with the course knowledge that applies to their daily job function.

Course Outline:
1. Introduction to Flip-Chip Technologies
2. UBM Metal Selection
3. Flip-Chip Solder Deposition Processes
4. Cu Pillar Bumping
5. C4 and Cu Pillar Fabrication Issues
6. Electromigration
7. Flip-Chip Plastic Ball Grid Array (FCPGA) Assembly Process Flow
8. Flip-Chip Ball Grid Array (FCBGA) Assembly Process Flow
10. Flip-Chip Si Package Co-Design and Chip-Package Interaction
11. Substrate Technologies, Underfill, Package Warpage Control, and Yield
12. Flip-Chip Reliability Assessment, Failure Modes, Examples, and Modeling

Who Should Attend:
The targeted audience includes scientists, engineers, and managers currently using flip-chip (with solder or Cu pillar) or those considering moving from wire bonding to flip-chip, as well as reliability, product or applications’ engineers who need a deeper understanding of flip-chip technologies: the advantages, limitations and failure mechanisms.

II. PACKAGE FAILURE ANALYSIS - FAILURE MECHANISMS AND ANALYTICAL TOOLS
Course Leaders: Rajen Dias – Amkor Technology and Deepak Goyal – Intel Corporation

Course Objectives:
The technical course will provide an overview of the failure modes and mechanisms observed in organic semiconductor packages. A brief introduction to the methodology of failure analysis for these packages will be described. The focus of the course will be on package failure mechanisms highlighted by case studies, analytical tools and techniques currently used, and the future direction for analytical tools and techniques required for successful and timely failure analysis of next generation package technologies. A discussion on the strategies for using these techniques and a flow chart for failure analysis will be included.

Course Outline:
1. Package Technology: Trends, Drivers and Challenges
2. Failure Analysis Challenges Offered by Package Technology Roadmaps
3. Introduction to the Methodology of Failure Analysis of Packages
4. Current Analytical Capabilities for Package Fault Isolation and Failure Analysis
5. Strategies to Use these Techniques to Identify Failures and Understand Failure Mechanisms
6. Analytical Capabilities to Support Next-Generation Packaging Technologies
7. Typical Failure Analysis Flow Charts for Opens and Shorts
8. Failure Modes/Mechanisms including Chip/Package Interactions, 1st/2nd Level Interconnections and Package/Board Substrates

Who Should Attend:
Engineers and technical managers who are involved in package technology development, reliability assessment of packages and failure analysis should attend.

12. 3D IC INTEGRATION AND 3D IC PACKAGING
Course Leader: John Lau – ASM Pacific Technology Ltd.

Course Objectives:
Recent advances in fan-out wafer/panel level packaging (TSMC’s InFO-WLP and Fraunhofer IZM’s FO-PLP), 3D IC packaging (TSMC’s InFO_PoP vs. Samsung’s ePoP), 3D IC integration (Hyundai’s HBM for AMD/Nvidia’s GPU vs. Micron’s HMC for Intel’s Knights Landing CPU), 2.5D IC Integration (TSV-less interconnects and interposers), embedded 3D hybrid integration, 3D CIS/IC integration, and 3D MEMS/IC integration will be discussed in this presentation. Emphasis is placed on various FO-WLP formation methods such as chip-first with die-up, chip-first with die-down, and chip-last (RDL-first). Since RDLs (redistribution layers) play an integral part of FO-WLP, various RDL fabrication methods such as Cu damascene, polymer, and PCB will be discussed. A few notes and recommendations on wafer vs. panel, dielectric materials, and molding materials will be provided. Also, TSV-less interposers such as those given by Xilinx/Spil, Amkor, Spil/Xilinx, ASE, MediaTek, Intel, TSMI, Shinko, Cisco/eSilicon, Sony’s TSV-less CIS, and Samsung/Hynix (HBM3) will also be discussed. Furthermore, new trends in semiconductor packaging will be presented.

Course Outline:
1. FOW/PLP: Chip-First (Die-Up/Down), Chip-Last (RDL-First)
2. RDL Fabrications: Polymer, PCB/LDI, Cu Damascene Methods
3. InFO-WLP, TSMC InFO-PoP vs. Samsung’s ePoP
4. Dielectric and Epoxy Mold Compound
5. Semiconductor and Packaging for IoTs (SiP)

Who Should Attend:
If you are involved with any aspect of the electronics/optoelectronic industry, you should attend this course. Each participant will receive more than 200 pages of handout materials from the lecturer’s books and the papers published by others.

13. FLEXIBLE HYBRID TECHNOLOGIES
Course Leader: Pradeep Lall – Auburn University

Course Objectives:
In this course, manufacture, design, assembly, and accelerated testing of flexible hybrid electronics for applications in some of the emerging areas will be covered. Flexible hybrid electronics opens the possibilities for the development of stretchable, bendable, foldable form factors in electronics applications which have been not possible with the use of rigid electronics technologies. Flexible electronics may be subjected to strain magnitudes in the neighborhood of 50-150 percent during normal operation. The integration processes and semiconductor packaging architectures for flexible hybrid electronics may differ immensely in comparison with those used for rigid electronics. The manufacture of thin electronic architectures requires the integration of thin-chips, flexible encapsulation, compliant interconnects, and stretchable inks for metallization tracks. A number of additive manufacturing processes for the fabrication and assembly of flexible hybrid electronics have become tractable. Processes for handling, pick-and-place operations of thin silicon and compliant interposers through interconnection processes such as reflow requires an understanding of the deformation and warpage processes for development of robust process parameters which will allow for acceptable levels of yields in high-volume manufacture. Modeling of operational stresses in flexible electronics requires the material behavior under loads including constant exposure to body temperature, salinity, sweat, ambient temperature, humidity, dust, wear and abrasion. The strain imposed on flexible stretchable electronics may far exceed those experienced in rigid electronics requiring the consideration of finite-strain
formulation in development of predictive models. The failure mechanisms, failure modes, acceleration factors in flexible electronics under operational loads of stretch, bend, fold and loads resulting from human body proximity are significantly different than rigid electronics. The testing, qualification and quality assurance protocols to meaningfully inform manufacturing processes and ensure reliability and survivability under exposure to sustained harsh environmental operating conditions, may differ in flexible electronics as well. A number of product areas for the application of flexible electronics are tractable in the near-term including Internet-of-Things (IoT), medical wearable electronics, textile woven electronics, robotics, communications, asset monitoring and automotive electronics.

Course Outline:
1. Ultra-Thin Chips
2. Die-Attach Materials for Flexible Semiconductor Packaging
3. Compliant Interconnects
4. Flexible Encapsulation Materials
5. Inkjet and Aerosol-Jet Printing Processes
6. Dielectric Materials for Large-Area Flexible Electronics
7. Flexible Substrates
8. Stretchable Inks for Printed Traces
9. Pick-and-Place and Material Handling Processes
10. Additive Technologies in Flexible Electronics
11. Reflow and Printing Processes
12. Accelerated Testing Protocols

Who Should Attend:
The course is intended to introduce the attendees to the general area of flexible hybrid electronics.

14. POLYMERS FOR ELECTRONIC PACKAGING
Course Leader: Jeffrey Gotro – InnoCentrix, LLC

Course Objectives:
The course will provide a broad overview of polymers used in semiconductor packaging and the important structure-property-process-performance relationships. We will cover in more depth the chemistries, material properties, and process considerations for adhesives, underfills, coatings and mold compounds. Additionally, we will provide an introduction to common thermal analysis methods (DSC, DMA, TMA, and TGA) used to characterize thermosetting polymers used in semiconductor packaging. Finally, the course will provide an introduction to the rheological performance of polymer-based materials used in packaging semiconductors. In most cases, adhesives, underfills, mold compounds and coatings are applied as a viscous liquid and then cured. The flow properties of these materials are critical to performance in high volume manufacturing. The course will provide an introduction to rheology measurements and examples of rheology issues in semiconductor packaging.

Course Outline:
1. Thermosetting Polymers Versus Thermoplastics
2. Temperature Dependence of Physical Properties
3. Thermosetting Polymers: Curing, Curing mechanisms, Network Formation
4. Overview of Key Chemicals Used: Epoxies, Acrylates, Polyimides, Bismaleimides
5. Chemistry of Die Attach Adhesives: Paste, Film and Wafer Applied
6. Chemistry and Physics of Capillary Underfills, Pre-Applied Underfills, Wafer Level Underfills,
7. Polymers used in Wafer Level Packaging, ewLP, and Other Fan-Out Packages
8. Packaging Substrate Materials and Process
9. Encapsulants (Mold Compounds) and Coatings
10. Introduction to Rheological Characterization Methods: Types of Rheometers and Basic Techniques
11. Introduction to the Rheological Properties of Adhesives
12. Key Rheology Properties: Shear Thinning, Viscosity, Rheology Changes during Curing

15. EMERGING INTERCONNECT AND SYSTEM INTEGRATION TECHNOLOGIES
Course Leader: Muhammad Bakir – Georgia Institute of Technology

Course Objectives:
Interconnects have emerged as a critical bottleneck to the realization of lower-power and higher-performance electronics. Coupled with this, the need for ever more tightly integrated systems presents unique cooling and power delivery challenges for next-generation electronics. This short course will present an overview of emerging technologies to address these need areas and present key modeling results to help guide technology development. The modeling effort presented in this short course will not only help us understand the design considerations of the technologies discussed but will also help benchmark the performance of the various technologies so that optimal systems can be developed.

Course Outline:
1. Advances in 2.5D Chip Integration, including Silicon-Bridge Based Approaches
2. 3D Integration Approaches, including Monolithic 3D ICs
3. Photonic Interposer and Package Technologies, including the Modeling of Diffusive Grating Couplers and the Impact of Misalignment
5. Advanced Cooling and Thermal Decoupling Technologies in Multi-Die Interconnected Systems, including Microfluidic Cooling
6. Mechanically Flexible Interconnects in Assembly of High-I/O Density Chips
7. Example Bioelectronic Systems Enabled by Advanced Interconnection and Packaging

Who Should Attend:
This short course will be of value to those working in the areas of interconnects, packaging, 3D technology, and heterogeneous integration.
profiles. High temperatures, random vibrations or humid and or wet environments affect system and materials. Lifetime demands of 10 years and above in combination with these challenging environments requires well known materials and broad knowledge on their behavior over the entire lifetime. Polymers are widely used in microelectronics packaging e.g. as interconnect material, encapsulant or substrate. But polymers age with time, temperature and humidity. Ageing entails a change in properties including mechanical, thermo-mechanical or adhesion characteristics, all of which are key factors for reliable package solutions. Hence, knowledge on materials and their ageing behavior is essential for developing reliable microelectronics packages and systems.

Course Outline:
1. Introduction of Polymers used in Microelectronics
2. Important Aspects of Encapsulation Technologies for Reliable Packaging
3. Ageing Mechanisms of Polymers
4. Adhesion and Interface Degradation
5. Test Methods and Selection Criteria for Polymers in Microelectronics Packaging
6. Overview of State-of-the-Art Measurement Equipment
7. Moisture and Temperature Induced Changes in Material Properties
8. Lifetime Simulation by FEM taking Polymer Degradation into Account
9. Failure Mechanisms Related to Polymer Ageing

Who Should Attend:
The course is targeted for engineers and engineer management in the field of microelectronic package design, development and reliability engineering. The attendees will learn about material selection, polymer ageing and the related influence on package reliability and will gain knowledge on how to build high reliable packages.

18. THERMO-ELECTRICAL CO-DESIGN FOR 3D INTEGRATION
Course Leaders: Ankur Srivastava - University of Maryland and Avram Bar-Cohen - Raytheon

Course Objectives:
3D integration of computational and RF components (in both homogeneous and heterogeneous combinations) provides significant improvements in functional efficiency, device density, and interconnect delays but is expected to lead to higher heat densities, along with decreased thermal management access to individual chips and on-chip hotspots. To fully achieve the inherent advantages of 3D integration it will, thus, be necessary to implement “embedded cooling” approaches and unify the thermal, mechanical, and electrical design of chip stacks and other integrated packaging configurations. Thermo-electro co-design for 3D integration is the theme of this CPMT Professional Development Course.

The PDC will begin with a brief review of 3D and 2.5D packaging form factors and the expected areal and volumetric heat extraction rates. It will be shown that conventional “remote cooling” techniques are incapable of meeting these thermal requirements, necessitating the use of “embedded cooling” solutions, including on-chip thermal vias, micro-fluidics, and thermoelectrics. Attention will then turn to creating an integrated co-design environment that will enable designers to perform the electrical-thermal-mechanical trade-offs needed to create computational and RF modules that achieve the highest functional throughput and efficiency. The PDC will close with presentation and discussion of several co-design case studies which demonstrate the added value of an integrated co-design environment. Co-Design for two distinct and significant integrated systems will be discussed: high performance computational modules and integrated Power Amplifier MMICs. For the computational modules we will discuss how greater performance and energy efficiency can be extracted by exploiting the unique interplay between power, performance and reliability for CPUs, ASICs and FPGA. For Power Amplifier MMICs we will discuss co-design techniques for generating greater gain, power-added efficiency (PAE), and output power thru the application of embedded cooling technologies.

Course Outline:
1. 3D/2.5D Packaging Trends
2. Embedded Cooling State-of-the-Art
3. Electronic Design Automation
4. Integrated Co-Design Environment
5. Thermo-Electrical Co-Design Case Studies: Computation
6. Thermo-Electrical Co-Design Case Studies: MMICs
7. Review and Lessons Learned

Who Should Attend:
The growing use of integrated co-design environments is blurring the line between IC designers and packaging engineers and creating a new class of EDA practitioners. This course will provide an introduction to this emerging EDA domain. The course is tailored to both IC designers and packaging engineers seeking to better understand the interplay between electrical and thermo-mechanical aspects of component design and how to best manage the trade-offs needed to achieve the highest functional throughput and efficiency in computational and RF components.

Continuing Education Units
The IEEE Components, Packaging and Manufacturing Technology Society (CPMT) is authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Professional Development Courses (PDCs) that will be presented at the 67th ECTC. CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in “non-credit” self-study courses, tutorials, symposia, and workshops. Complete details, including voluntary enrollment forms, will be available at the conference. All costs associated with ECTC Professional Development Course CEUs will be underwritten by the conference, i.e., there are no additional costs for Professional Development Course attendees to obtain CEU credit.

IMPORTANT NOTICE
Morning PD Courses 1 through 9 or afternoon PD Courses 10 through 18 run concurrently. Make sure you indicate specific course numbers you plan to attend when you register online. See page 30 for registration information.

AREA ATTRACTIONS
In the heart of the Walt Disney World® Resort, the award-winning Walt Disney World Swan and Dolphin Resort is your gateway to Central Florida’s greatest theme parks and attractions. The resort is located between Epcot ® and Disney’s Hollywood Studios ™, and nearby Disney’s Animal Kingdom ™ Theme Park and Magic Kingdom ® Park.

Come discover our 17 world-class restaurants and lounges, sophisticated guest rooms with Westin Heavenly Beds® and the luxurious Mandara Spa. Enjoy five pools, two health clubs, tennis, nearby golf, and many special Disney benefits, including complimentary transportation to Walt Disney World theme parks and attractions and the Extra Magic Hours benefit.

Just minutes from the Walt Disney World Swan and Dolphin Resort is Downtown Disney® West Side and Marketplace. Downtown Disney’s West Side showcases top-notch restaurants, a 24-screen AMC Pleasure Island movie theater, and other uncommon shops. Here you’ll also find the exquisite Cirque du Soleil La Nouba live entertainment show and the DisneyQuest Indoor Interactive theme park.

Downtown Disney Marketplace provides an appealing place to take a break from Disney theme parks and water parks. Check out the largest Disney character store in the world. Or, for more of a respite, relax and dine at a lakeside restaurant.

Should you decide to explore outside the greater Lake Buena Vista area, Orlando boasts other parks and recreation areas tailor made for your pleasure. Favorites include Universal Orlando, SeaWorld, Gatorland, and Winter Park.
## Program Sessions: Wednesday, May 31, 8:00-11:40 a.m.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Committee: Advanced Packaging</td>
<td>Committee: Interconnections</td>
<td>Committee: Assembly &amp; Manufacturing Technology</td>
</tr>
</tbody>
</table>

### Session Co-Chairs:

- Beth Keser – Intel Corporation
- Email: keser@intel.com

### Mike Ma – Amkor Technology Taiwan (ATT)
- Tel: +886-975-778628
- Email: mike.ma@amkor.com

### Yoichiro Sato – Asahi Glass Company; Lutz Parthier – Fraunhofer IZM; Markus Wöhrmann; Steve Voges; and Klaus-Dieter Lang – Technical University Berlin; Matthias Wietstruch and Mehmet Kaynak – IHP Microelectronics

### Tanja Braun, Stefan Raatz, Marius van Dijk; Karl-Friedrich Becker; and Rolf Aschenbrenner – Fraunhofer IZM; Markus Wöhrmann; Steve Voges; and Klaus-Dieter Lang – Technical University Berlin; Matthias Wietstruch and Mehmet Kaynak – IHP Microelectronics

### Tailong Shi, Vanessa Smet, Venky Sundaram, and Esperanza Torres – Electronics Research Alliance (ERA) ...

### Session 1: Fan-Out Packaging Process and Integration

1. **8:00 AM - Development of a Multi-Project Fan-Out Wafer Level Packaging Platform**
   - Tanja Braun, Stefan Raatz, Marius van Dijk; Karl-Friedrich Becker; and Rolf Aschenbrenner – Fraunhofer IZM; Markus Wöhrmann; Steve Voges; and Klaus-Dieter Lang – Technical University Berlin; Matthias Wietstruch and Mehmet Kaynak – IHP Microelectronics

2. **8:25 AM - SLIM™, High-Density Wafer Level Fan-Out Package Development with Submicron RDL**
   - Youngrae Kim, Jann-Hun Bae, Min-Hwa Chang, AhRa Jo, Ji Hyun Kim, SangMun Park, David Hiner, Mike Kelly, and WonChul Do – Amkor Technology

3. **8:50 AM - Development of Novel High-Density System Integration Solutions in FOWLP – Complex and Thin Wafer-Level SIP and Wafer-Level 3D Packages**
   - Andre Cardoso, Alberto Martinis, Hugo Barros, Eleabete Fernandes, Abel Janeiro, and Eoin O’Toole – NANIUM

### Session 2: TSV Process, Characterization and Applications

1. **8:00 AM - A Cost-Effective Via Last TSV Technology Using Molten Solder Filling for Automobile Application**
   - Yuki Ohara, Yuki Inagaki, Masaki Matsui, and Kazushi Asami – DENSO

2. **8:25 AM - Accurate Depth Control of Through-Silicon Via by Substrate Integrated Etch Stop Layers**
   - Matthias Wietstruch, Steffen Marschmeyer, Marco Lisker, Andreas Krueger, Dirk Wolansky, Philipp Kulse, Alexander Goenitz, Thomas Voss, Andreas Mai, and Mehmet Kaynak – IHP; Mesut Inac – Technical University Berlin

3. **8:50 AM - Application of a Metallic Copper Cap Layer to Control Cu TSV Extrusion**
   - Golareh Jalalvand, Omar Ahmed, Keenan Bosworth, Zherlin Fei, Cullen Fitzgerald, and Tengfei Jiang – University of Central Florida

### Session 3: Flip Chip Assembly

4. **10:00 AM - Thermal-Compression Bonding and Mass Reflow Assembly Processes of 3D Logic Die Stacks**
   - Pascale Gagnon, Christian Bergeron, Richard Langlois, Stéphane Barbeau, Steve Whitehead, Kazushige Sakuma, Raphael Robertazzi, and Christy Tyberg – IBM Corporation

5. **10:25 AM - Chip Shooter to Enable Fine Pitch Flip Chip**
   - Jie Fu, Manuel Adreite, and Milind Shad – Qualcomm Technologies, Inc.

### Refreshment Break: 9:15-10:00 a.m.

   - Dazuan Yu, Zhiyi Xiao, Li Yang, Min Xiang – Huatian Technology

7. **11:15 AM - First Demonstration of Panel Glass Fan-Out (GFO) Packages for High I/O Density and High-Frequency Multi-Chip Integration**
   - Tailong Shi, Vanessa Smet, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Yoichiro Sato – Asahi Glass Company; Lutz Partner – SCHOTT; Frank Wei and Cody Lee – DISCO

8. **11:15 AM - Fine Pitch Interconnect Rework for Lead-Free Flip Chip Packages**
   - Malak Kanso, David Danovitch, and Bode Nguena – Sherbrooke University; Richard Langlois and Christian Bergeron – IBM Corporation
### Program Sessions: Wednesday, May 31, 8:00-11:40 a.m.

<table>
<thead>
<tr>
<th>Session 4: Advanced Substrates and Integrated Devices</th>
<th>Session 5: Emerging Sensors and Microsystems Packaging</th>
<th>Session 6: 5G, mmWave and Beyond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Committee: Materials &amp; Processing</td>
<td>Committee: Emerging Technologies</td>
<td>Committee: High-Speed, Wireless &amp; Components</td>
</tr>
<tr>
<td>Session Co-Chairs: Tiejun Zheng – Microsoft Corporation Tel: +1-425-722-1141 Email: <a href="mailto:tzheng@microsoft.com">tzheng@microsoft.com</a> Dwayne Shirley</td>
<td>Session Co-Chairs: Bharat Penmecha – Intel Corporation Tel: +1-480-552-2511 Email: <a href="mailto:bharrat.penmecha@intel.com">bharrat.penmecha@intel.com</a> Ramakrishna Kotlanka – Analog Devices Tel: +1-781-937-1076 Email: <a href="mailto:rama.krishna@analog.com">rama.krishna@analog.com</a></td>
<td>Session Co-Chairs: Kemal Aygun – Intel Corporation Tel: +1-480-552-1740 Email: <a href="mailto:kemal.aygun@intel.com">kemal.aygun@intel.com</a> Li-Hong Hwang – National Sun Yat-Sen University Tel: +886-7-5252000 ext. 4485 Email: <a href="mailto:FiftyOhm@mail.nsysu.edu.tw">FiftyOhm@mail.nsysu.edu.tw</a></td>
</tr>
<tr>
<td>1. 8:00 AM - Novel Organic Substrates with Enhanced Thermal Conductivity Xiaoliang Zeng, Jiajia Sun, and Rong Sun – Shenzhen Institutes of Advanced Technology; Jianbin Xu and Ching-Ping Wong – Chinese University Hong Kong</td>
<td>1. 8:00 AM - Phototriggerable, Transparent Electronics: Component and Device Fabrication Gerald Goudin, Oluwadamilola Phillips, Jared Schwartz, Anthony Engler, and Paul Kohl – Georgia Institute of Technology</td>
<td>1. 8:00 AM - First Demonstration of 28GHz and 39GHz Transmission Lines and Antennas on Glass Substrates for 5G Modules Atom Watanabe, Muhammad Ali, Bjarne Taheri, Jimmy Hester, Markondeya Pulugurtha, Venky Sundaram, Manos Tentzeris, and Rao Tummala – Georgia Institute of Technology; Hiroyuki Matsuura – NGK Spark Plug; Tomonori Ogawa – Asahi Glass</td>
</tr>
<tr>
<td>3. 8:50 AM - Development of Solder Resist with Improved Adhesion at HTSL (175°C for 3000 Hours) for Automotive IC Package Nobuhito Itto – Taiyo Ink</td>
<td>3. 8:50 AM - Atomically Thin Vertical van der Waals Heterostructure for Broadband Photodetection Bo Sun, Tielin Sh, Youyi Wu, Jianxin Zhou, Zirong Tang, and Guangfan Liao – Huazhong University of Science &amp; Technology</td>
<td>3. 8:50 AM - Fabrication of Terahertz Components using Aerosol-Jet Printing Christopher Oakley, Amanpreet Kaur, Jennifer Byford, and Premjeet Chahal – Michigan State University</td>
</tr>
<tr>
<td>Refreshment Break: 9:15-10:00 a.m.</td>
<td>4. 10:00 AM - Bondable Copper Substrates with Silver Solid Solution Coating for High-Power Electronic Applications Yongjun Huo and Chin C. Lee – University of California, Irvine</td>
<td>4. 10:00 AM - High-Performance Chip-Partitioned Millimeter Wave Passive Devices on Smooth and Fine Pitch InFO RDL Che-Wei Hsu, Chung-Hao Tsai, Jeng-Shen Hsieh, Kuo-Chung Yee, Chue-Tang Wang, and Douglas Yu – Taiwan Semiconductor Manufacturing Company, Ltd.</td>
</tr>
<tr>
<td>4. 10:00 AM - Fractal-Structured, Wearable Soft Sensors for Control of a Robotic Wheelchair via Electrooculograms Saswat Mishra, Nicolas Agee, Yongkuk Lee, Dong Sup Lee, and Woobong Yeo – Virginia Commonwealth University; James J. S. Norton – University of Illinois at Urbana-Champaign</td>
<td>5. 10:25 AM - Fractal-Structured, Wearable Soft Sensors for Control of a Robotic Wheelchair via Electrooculograms Saswat Mishra, Nicolas Agee, Yongkuk Lee, Dong Sup Lee, and Woobong Yeo – Virginia Commonwealth University; James J. S. Norton – University of Illinois at Urbana-Champaign</td>
<td>5. 10:25 AM - Directional Through Glass Via (TGV) Antennas for Wireless Point-to-Point Interconnects in 3D Integration and Packaging Sehee Hwangbo, Hyowon Ar, Sheng-Po Fang, and Yong-Kyu Yoon – University of Florida; Aric B. Shorey and Abbas M. Kazmi – Corning, Inc.</td>
</tr>
<tr>
<td>7. 11:15 AM - Passive Device for RF Application Yanifei Chen, Stephanie Greene, Puneeth Shridhar, and Youngjia Chun – University of Pittsburgh; Connor Howe and Woobong Yeo – Virginia Commonwealth University; Emery Stephen – Magee-Womens Hospital of UPMC</td>
<td>8. 50 AM - Development of Solder Resist with Improved Adhesion at HTSL (175°C for 3000 Hours) for Automotive IC Package Nobuhito Itto – Taiyo Ink</td>
<td>8. 50 AM - Development of Solder Resist with Improved Adhesion at HTSL (175°C for 3000 Hours) for Automotive IC Package Nobuhito Itto – Taiyo Ink</td>
</tr>
<tr>
<td>-----------------------------------------------</td>
<td>---------------------------------------------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td><strong>Committee:</strong> Advanced Packaging</td>
<td><strong>Committee:</strong> Assembly &amp; Manufacturing Technology</td>
<td><strong>Committee:</strong> Interconnections</td>
</tr>
<tr>
<td><strong>Session Co-Chairs:</strong></td>
<td><strong>Session Co-Chairs:</strong></td>
<td><strong>Session Co-Chairs:</strong></td>
</tr>
<tr>
<td>Tel: +1-518-222-1860</td>
<td>Tel: +1-410-765-7859</td>
<td>Tel: +1-450-534-8000 X-1400</td>
</tr>
<tr>
<td>Email: <a href="mailto:luke.englund@globalfoundries.com">luke.englund@globalfoundries.com</a></td>
<td>Email: <a href="mailto:Garry.Cunningham@ngc.com">Garry.Cunningham@ngc.com</a></td>
<td>Email: <a href="mailto:David.Danovitch@USherbrooke.ca">David.Danovitch@USherbrooke.ca</a></td>
</tr>
<tr>
<td>Bora Baloglu – Amkor Technology</td>
<td>Li Jiang – Texas Instruments, Inc.</td>
<td>Li Li – Cisco Systems, Inc.</td>
</tr>
<tr>
<td>Tel: +1-480-786-7307</td>
<td>Tel: +1-214-479-4537</td>
<td>Tel: +1-408-527-0801</td>
</tr>
<tr>
<td>Email: <a href="mailto:bora.baloglu@amkor.com">bora.baloglu@amkor.com</a></td>
<td>Email: <a href="mailto:ljjiang@ti.com">ljjiang@ti.com</a></td>
<td>Email: <a href="mailto:LlLi2@cisco.com">LlLi2@cisco.com</a></td>
</tr>
<tr>
<td><strong>1. 1:30 PM - A Novel Multi-Layer Film Type</strong></td>
<td><strong>1. 1:30 PM - Development of Low Power</strong></td>
<td><strong>1. 1:30 PM - Cu-SnAg Interconnects</strong></td>
</tr>
<tr>
<td><strong>Interconnection Substrate</strong></td>
<td><strong>Stealth Laser for Thick Die As A Solution</strong></td>
<td><strong>Evaluation for the Assembly at 10µm and</strong></td>
</tr>
<tr>
<td>Chih-Kuang Yang – Princo Corporation</td>
<td><strong>for Protective Overcoat Damage</strong></td>
<td><strong>5µm Pitch</strong></td>
</tr>
<tr>
<td></td>
<td>Jeniffer Aspura, Jessa Resol, and Roderick Balares –</td>
<td>Divya Tanega, Marion Volpert, Gilles Lasargues, Boris</td>
</tr>
<tr>
<td></td>
<td>Texas Instruments, Inc.</td>
<td>Boullard, Aurelie Vandenee, Tank Chars, Yannick Goiran, and David Henry – CEA-Leti; Fiqui-Hodaj –</td>
</tr>
<tr>
<td></td>
<td></td>
<td>University Grenoble Alps, SIMaP Laboratory</td>
</tr>
<tr>
<td><strong>2. 1:55 PM - Ultra-Low Temperature</strong></td>
<td><strong>2. 1:55 PM - Laser Multi Beam Full Cut</strong></td>
<td><strong>2. 1:55 PM - Scaling Cu Pillars to 20µm</strong></td>
</tr>
<tr>
<td><strong>FOWLP Process for the Embedding of Low</strong></td>
<td><strong>Dicing of Wafer Level Chip-Scale Packages</strong></td>
<td><strong>Pitch and Below: Strategic Role of Surface</strong></td>
</tr>
<tr>
<td><strong>Thermal Budget Sensors and Components</strong></td>
<td>Jeroen van Borkulo, Eric Tan, and Richard van der Stam – ASM</td>
<td><strong>Finish and Barrier Layers</strong></td>
</tr>
<tr>
<td><strong>Using SU-8 as Dielectric</strong></td>
<td>Pacific Technologies</td>
<td>Ting-Chia Huang, Vanessa Smet, Plulugurtha</td>
</tr>
<tr>
<td>Raquel Pinto, André Cardoso, Sara Ribeiro, and Carlos Brandão – NANNUM: João Gaspar, Rizwan Gill, Holder Fonseca, and Margaret Costa – INL, Filipe Cardoso and Manana Antunes – MAGNOMICS</td>
<td>Markondeya Raj, and Rao Tummalra – Georgia Institute of Technology; Robin Taylor, Gustavo Ramos, Rick Nichols, and Aim Kilan – Atotech</td>
<td></td>
</tr>
<tr>
<td><strong>3. 2:20 PM - Integrated Copper Heat Slugs</strong></td>
<td><strong>3. 2:20 PM - Plasma Dicing 300mm Framed</strong></td>
<td><strong>3. 2:20 PM - Thermal Compression Bonding:</strong></td>
</tr>
<tr>
<td>and EMI Shields in Panel Laminated Fanout (LO)</td>
<td>Wafers - Analysis of Improvement in Die Strength and Cost Benefits for Thin Die Singulation</td>
<td>Understanding Heat Transfer by in situ Measurement and Modeling</td>
</tr>
<tr>
<td><strong>(LFO) and Glass Fanout (GFO) Packages</strong></td>
<td>Richard Barnett, Oliver Ansell, Martin Hanicin, Janet Hopkins, Joanne Carpenter, William Worzter, and Carolyn Short – SPTS Technologies</td>
<td>Peter Bex, Teng Wang, Vladimir Cheman, Melina Lofrano, Giovanni Capuz, Erik Sleekoe, and Eric Beyne – IMEC</td>
</tr>
<tr>
<td><strong>for High-Power RF ICs</strong></td>
<td></td>
<td><strong>4. 3:30 PM - A Study on Nano-sized Silica</strong></td>
</tr>
<tr>
<td>Verly Sundaram, Baret Digospro, Nahid Gagin, P. Markondeya Raj, and Rao Tummalra – Georgia Institute of Technology; Kyle Byers and Sean Garrison – Honeywell; Garth Kraus and Michael Bishby – Sanda National Laboratories</td>
<td><strong>Content and Size Effect in Non Conductive Films (NCFs) for Ultra Fine-Pitch Cu-Pillar/Sn-Ag Micro-Bump Interconnection</strong></td>
<td>HanMin Lee, SeYong Lee, SeMin Cho, Younghyun Yu, Jong-Ho Park, and Kyung-Wook Paik – Korea Advanced Institute of Science &amp; Technology</td>
</tr>
<tr>
<td><strong>4. 3:30 PM - Implementation of Thick</strong></td>
<td><strong>4. 3:30 PM - Plasma Dicing Fully Integrated</strong></td>
<td><strong>5. 3:55 PM - Accelerated SLID Bonding for Fine-Pitch Interconnects with Porous Microstructure</strong></td>
</tr>
<tr>
<td><strong>Copper Inductor Integrated into Chip Scaled</strong></td>
<td><strong>Process-Flows Suitable for BEOL Advanced</strong></td>
<td>Jörg Meyer, Juliana Panchenko, and Steffen Bickel – Technical University Dresden; Wieland Wahrmund and M. Jürgen Wolf – Fraunhofer IZM, ASSID</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td><strong>Dicing Fabrications</strong></td>
<td><strong>6. 4:20 PM - Low-Temperature Ni/Sn/Ni</strong></td>
</tr>
<tr>
<td>Sheng-Bin Yang, C. C. Chen, W. L. Huang, T. L. Yang, C. L. Chang, H.L. Huang, C. C. Chou, C. Y. Ku, C. S. Chen, and Alexander Kalntisky – Taiwan Semiconductor Manufacturing Company, Ltd.</td>
<td><strong>Transient Liquid Phase Bonding for High Temperature Packaging Application by Imposing Temperature Gradient</strong></td>
<td>Yi Zhong, Wei Dong, Mingliang Huang, Hatao Ma, and Ning Zhao – Dalan University of Technology; C. P. Wong – Georgia Institute of Technology</td>
</tr>
<tr>
<td><strong>5. 3:55 PM - Passive Devices Fabrication</strong></td>
<td><strong>5. 5:55 PM - Stealth Dicing Challenges for</strong></td>
<td><strong>7. 4:45 PM - Additive Manufacturing of</strong></td>
</tr>
<tr>
<td><strong>on FOWLP and Characterization for RF</strong></td>
<td><strong>MEMS Wafer Applications</strong></td>
<td><strong>Centric Components for Heterogeneous Integration</strong></td>
</tr>
<tr>
<td><strong>6. 4:20 PM - Organic versus Inorganic RDL</strong></td>
<td><strong>6. 4:20 PM - A Novel Pick-Up and Place</strong></td>
<td><strong>7. 4:45 PM - Investigation of Production</strong></td>
</tr>
<tr>
<td><strong>Dielectrics for High-Performance Graphics</strong></td>
<td><strong>Process for FOWLP Using Tape Expansion</strong></td>
<td><strong>Quality and Reliability Risk of ELK Wafer</strong></td>
</tr>
<tr>
<td>Applications**</td>
<td><strong>Machine Device</strong></td>
<td><strong>WLCSP Package</strong></td>
</tr>
<tr>
<td><strong>7. 4:45 PM - Additive Manufacturing</strong></td>
<td><strong>7. 4:45 PM - Investigation of Production</strong></td>
<td><strong>Interfacial Reaction and Microstructural Evolution Between Au-Ge Solder and Electroless Ni-W-Co Metallisation in High-Temperature Electronics Interconnects</strong></td>
</tr>
<tr>
<td><strong>Centric Components for Heterogeneous Integration</strong></td>
<td><strong>Quality and Reliability Risk of ELK Wafer</strong></td>
<td>Li Liu – Wuhan University of Technology; Jie Cui – Auburn University; Jing Wang, Zhaoxia Zhou, and Chaoqin Liu – Loughborough University; R. Wayne Johnson – Tennessee Tech University</td>
</tr>
<tr>
<td>Yi Yan, Lanbing Liu, and Guo-Quan Lu – Virginia Tech; Lus Nguyen and Jim Moss – Texas Instruments, Inc.; Yunkui Mei – Tianjin University</td>
<td><strong>WLCSP Package</strong></td>
<td><strong>17</strong></td>
</tr>
</tbody>
</table>

**Program Sessions: Wednesday, May 31, 1:30-5:10 p.m.**
1. 1:30 PM - Hybrid Approach to Conduct Failure Prognostics of Automotive Electronic Control Unit
Bulong Wu, Dae-Suk Kim, and Bongtae Han – University of Maryland; Alicja Palczynska, Prazmyslaw Jakub Gromala, and Alexandru Prisacaru – Robert Bosch

2. 1:55 PM - Visualization of Microstructural Evolution in Lead-Free Solders During Isothermal Aging Using Time-Lapse Imagery
Sudan Ahmed, Nianjun Fu, Jeffrey Suhling, and Pradeep Goyal – Intel Corporation

3. 2:20 PM - Correlation of Dielectric Film Flex Fatigue Resistance and Package Resin Cracking Failure
Joseph Ross, Nicolas Pizzuti, Steven Ostrander, and Kamal Sikka – IBM Corporation

4. 3:30 PM - Development of FE Models and Measurement of Internal Deformations of Fuze Electronics Using X-Ray MicroCT Data with Digital Volume Correlation
Pradeep Lall and Nakul Kothari – Auburn University; John Deep and Jason Foley – US Air Force Research Labs; Ryan Lowe – ARA Associates

5. 3:55 PM - Dynamic Stress Measurements of Electronic Devices During Active Operation
Markus Fesst, Elke Moeller, Andi Wijaya, and Juergen Wilde – University of Freiburg, IMTEK; Johanna Ocklenburg – Infineon Technologies

6. 4:20 PM - Smart Packaging: A Micro-Sensor Array Package to Investigate the Effect of Humidity in Microelectronic Packages
Aurore Quellenec, Umar Shafique, and Dominque Drouin – Université de Sherbrooke; Eric Duchesne – IBM Corporation; Hélène Frémont – Université de Sherbrooke; Éric Duchesne – Université de Sherbrooke; and Olivier Castany – CEA-Leti; Philippe Arguel – CNRS

7. 4:45 PM - Nondestructive, In Situ Mapping of Die Surface Displacements in Encapsulated IC Chip Packages using X-Ray Diffraction Imaging Techniques
Nima E. Gorji, Rajani K. Vijayaraghavan, and Patrick J. McNally – Dublin City University; Brian K. Tanner – Durham University; Andreas N. Danilewsky – Albert Ludwigs University

1. 1:30 PM - Effect of Processing Variables on the Mechanical Reliability of SnAg/Cu Pillar Solder Joints
Mohammed Genanu, Babak Arfaei, and Eric Coste – Binghamton University; Francis Mutuku and James Wilcox – Universal Instruments; Eric Perfecto – GLOBALFOUNDRIES

2. 1:55 PM - Visualization of Microstructural Evolution in Lead-Free Solders During Isothermal Aging Using Time-Lapse Imagery
Sudan Ahmed, Nianjun Fu, Jeffrey Suhling, and Pradeep Goyal – Intel Corporation

3. 2:20 PM - Failure Mechanism and Kinetics Studies of Electroless Ni-P Dissolution in Pb-Free Solder Joints under Electromigration
Pilin Liu, Alan Overson, Chaitra Chavali, and Deepak Lall – Auburn University

4. 3:30 PM - Optoelectronic Chip Assembly Process of Optical MCM
Masao Tokunari, Koji Masuda, Hsang-Han Hsu, Takashi Hisada, Shigeru Nakagawa, Richard Langlois, Patrick Jacques, and Paul Fortier – IBM Corporation

5. 3:55 PM - 3D Packaging of Embedded Optoelectronic Die and CMOS IC Based on Wet Etched Silicon Interposer
Chenhui Li, Alain Molnar, Teng Li, Ripalita Stabile, and Oded Raz – Eindhoven University of Technology

6. 4:20 PM - Self-Alignment with Copper Pillars Micro-Bumps for Positioning Optical Devices at Submicron Accuracy
Yézouma Dieudonné Zonou, Stéphane Bernabe, and Olivier Castany – CEA-Leti; Philippe Arguel – Laboratory for Analysis and Architecture of Systems, CNRS

7. 4:45 PM - Thermal Management Characterization of Microassembled High-Power Distributed-Feedback Broad Area Lasers Emitting at 975nm
Roberto Mostallino, Michel Garcia, Alexandre Larrue, Yannick Robert, Eric Vinet, Michel Leconte, Olivier Parlialaud, and Michel Krakowski – III-V Lab; Yannick Deshayes and Laurent Bechou – University of Bordeaux
Session 13: Interconnect Advances in FO & WLP

Committee: Interconnections

1. 8:00 AM - SLIM™ Advanced Fan-Out Packaging for High Performance Multi-Die Solutions
   Young Rae Kim and Won Chul Do – Amkor Technology

2. 8:25 AM - 28nm CPI (Chip/Package Interactions) in Large Size eWLB (Embedded Wafer Level BGA) Fan-Out Wafer Level Packages
   Yaqian Lin – STATS ChipPAC

3. 8:50 AM - Multi DOE Study on 28nm (RF) WLP Package to Investigate BLR Performance of Large WLP Die with 0.35mm Ball Pitch Array
   Rey Alvarado, Beth Keser, Tong Cui, and Ahnmer Syed – Qualcomm Technologies, Inc.

4. 10:00 AM - Warpage and Thermal Optimization of Fan-Out Wafer/Panel-Level Packaging
   John Lau, Ming Li, DeWen Tian, Nelson Fan, Eric Kuah, and Eric Ng – ASMT International; Zhang Li and Kim Hwee Tan – Janggun Changdian Advanced Packaging Co., Ltd.; Rozalia Beica – Dow Chemical; Yu-Hua Chen – Unimicron

5. 10:25 AM - A Novel 3D IC Wafer-level Package for New Wave MEMS
   Uwe M Hansen, Ralf Reichenbach, David Polityko, and Sebastian Schuler-Watkins – Robert Bosch; Che-Hau Huang, Yung-Hui Wang, and Ying-Teu Ou – Advanced Semiconductor Engineering, Inc.

6. 10:50 AM - UBM/RDL Deposition by PVD for FOWLP in High-Volume Production
   Chris Jones, Stephen Burgess, Tony Wilby, Paul Densley, David Butler, and Carolyn Short – SPTS Technologies

7. 11:15 AM - Reliability of Large Fan-Out Wafer Level Package Based Package-on-Package
   Srinivasa Rao Vempati, David Ho, Mian Zhi Ding, Se Choong Chong, Sharon Lim PS, and Tai Chong Chai – Institute of Microelectronics, A*STAR

Session 14: Heterogeneous Integration

Committees: Advanced Packaging joint with Assembly & Manufacturing Technology

1. 8:00 AM - A Versatile Platform Towards High Reliability Compact Package for Digital Chips
   Christine Ferrandin, Laetitia Castagné, Braham Kholti, Guillaume Wilterman, Vincent Puyal, Romain Lemaire, Fabrice Casset, Gilles Simon, and Jean-Charles Soursou – CEA-Leti; Lionel Toffanin and Sébastien Petitdidier – ST Microelectronics

2. 8:25 AM - Glass Based 3D-IPD Integrated RF ASIC in WLCSP

3. 8:50 AM - Breakthrough in Cu to Cu Pillar-Concave Bonding on Silicon Substrate with Polymer Layer for Advanced Packaging, 3D, and Heterogeneous Integration
   Yu-Tao Yang, Ting-Yang Yu, Shu-Chao Kuo, and Kuan-Neng Chen – National Chiao Tung University; Tai-Yuan Huang, Kai-Ming Yang, Cheng-Ta Ko, Yu-Hua Chen, and Tzyy-Jang Tseng – Unimicron

4. 10:00 AM - Heterogeneous Interposer Based Integration of Chips with Copper Pillars and C4 Balls to Achieve High-Speed Interfaces for ADC Application
   Andy Henig, Fabina Hopsch, Robert Fischbach, Michael Dittrich, and Robert Trieb – Fraunhofer IIS/ EAS

5. 10:25 AM - “FlexTrate®” – Scaled Heterogeneous Integration on Flexible Biocompatible Substrates
   Tak Fukushima, Mirco Marz in, Saptadeep Pal, Zhe Wan, Siva Jangam, Anirudh Sathe, Adeel Baija, and Subramanian Iyer – University of California, Los Angeles

6. 10:50 AM - Metal Contamination Evaluation of Via-Last Cu TSV Process Using Notchless Si Etching and Wet Cleaning of the First Metal Layer
   Naoya Watanabe, Haruo Shimamoto, Katsuya Kikuchi, and Masahiro Aoyagi – AIST; Hidekazu Kikuchi, Azusa Yanagisawa, and Akio Nakamura – LAPIS Semiconductor

7. 11:15 AM - A Highly Miniaturized System Integration Approach for an IOT Contactless Power Module
   Srikrisna Shiramani, Tony Contreras, Jian Wang, Mingjie Fan, Minjie Chen, Yuming Song, and Terry Bowen – Tyco Electronics

Session 15: Flip Chip and Embedding in Substrates

Committee: Advanced Packaging

1. 8:00 AM - Solder Mobility for High-Yield Self-Aligned Flip-Chip Assembly
   Yves Martin, Swetha Kamalupurk, Jae-Woong Nah, Nathan Marchick, and Tymon Barwicz – IBM Corporation

2. 8:25 AM - Large Scale Cryogenic Integration Approach for Superconducting High-Performance Computing
   Rabindra Das, Vladimir Bolkhovsky, Sergey Tolpygo, Pascale Gouker, Leonard Johnson, Eric Dauler, and Mark Gouker – MIT Lincoln Laboratory

3. 8:50 AM - Compressible MicroInterconnects (CMIs) for Heterogeneous Microsystem Integration
   Paul Jo, Muneeb Zia, Joe Gonzalez, and Muhammad Bakir – Georgia Institute of Technology

4. 10:00 AM - Package Design Considerations and Coupling from Embedded Passive Inductors
   Jan Liu, Janani Chandrasekhar, Andrew Collins, Hui Liu, and Guang Chen – Intel Corporation

5. 10:25 AM - Advanced Embedded Package for Power Devices
   Naoki Hayashi, Miki Nakashima, Hiroaki Matsubara, Hiroshi Demachi, Shingo Nakamura, Tomoshige Chikai, Fumihiko Taniguchi, Yukari Imaizumi, Yoshikiko Ikemoto, Mitsu Ooida, and Akito Yoshida – J-Devices

6. 10:50 AM - Development of Large Size CPU Package Structure using Embedded Thin Film Capacitor Package Substrate
   Masatomo Kaise, Kenji Fukuzono, Manabu Watanabe, Daisuke Mizutani, Tomoyuki Akahoshi, Hidehiko Fujisaki, Seigo Yamawaki, and Kei Fukui – Fujitsu Semiconductor

   Angela Kessler, Andreas Munding, Thorsten Scharf, Boris Pilkat, and Klaus Pressel – Infineon Technologies

Session Co-Chairs:
Lei Shan – IBM Corporation
Tel: +1-914-945-3200
Email: lei@us.ibm.com

Dingyou Zhang – Qualcomm Technologies, Inc.
Tel: +1-858-845-5905
Email: zhangdingyou04@gmail.com

Email: leis@us.ibm.com
Tel: +1-914-945-3306
Email: knickerj@us.ibm.com

Email: stffen.kroehnert@nanium.com
Tel: +43-676-8955-4087
Email: steffen.kroehnert@nanium.com

Email: m.leitgeb@ats.net
Tel: +43-676-8955-4087
Email: m.leitgeb@ats.net

Email: chunho.kim@medtronic.com
Tel: +1-480-377-3664
Email: chunho.kim@medtronic.com

Email: knickerj@us.ibm.com
Tel: +1-914-945-3306
Email: knickerj@us.ibm.com

Session Co-Chairs:
John Knickerbocker – IBM Corporation
Tel: +1-914-945-3306
Email: knickerj@us.ibm.com

Chunho Kim – Medtronic Corporation
Tel: +1-800-377-3664
Email: chunho.kim@medtronic.com

Session Co-Chairs:
John Knickerbocker – IBM Corporation
Tel: +1-914-945-3306
Email: knickerj@us.ibm.com

Steffen Kroehnert – Nanium S.A.
Tel: +49-171-5639472
Email: steffen.kroehnert@nanium.com

Session Co-Chairs:
Markus Leitgeb – AT&SF
Tel: +43-676-8955-4087
Email: m.leitgeb@ats.net

Email: steffen.kroehnert@nanium.com
Tel: +49-171-5639472
Email: steffen.kroehnert@nanium.com

Program Sessions: Thursday, June 1, 8:00-11:40 a.m.

Refreshment Break: 9:15-10:00 a.m.
# Program Sessions: Thursday, June 1, 8:00-11:40 a.m.

## Session 16: 3D Materials and Processing

**Committee:** Materials & Processing  
**Session Co-Chairs:**  
Myung Jin Yim – Intel Corporation  
Tel: +1-408-728-1393  
Email: myungjin.yim@intel.com  
Mikel Miller – Draper Laboratory  
Tel: +1-617-258-2844  
Email: mmiller@draper.com

### 1. 8:00 AM - Highly Productive 3D Stacking Process
Kazutaka Honda, Hiroshi Onozeki, and Shizu Fukuzumi – Hitachi Chemical

### 2. 8:25 AM - Direct Bonding and Debonding Approach of Ultrathin Glass Substrates for High-Temperature Devices
Messaoud Bedjaoui and Sylvan Poulet – CEA-Leti

### 3. 8:50 AM - Wafer-Level Vacuum-Packaged Piezoelectric Energy Harvesters Utilizing Two-Step Three-Wafer Bonding
Nan Wang, Chengfang Sun, Li Tan, Siow, Hong Miao Ji, Darmayuda I Made, Peter Hyun Kee Chang, Qing Xin Zhang, and Yuandong Gu – Institute of Microelectronics, A*STAR

### 4. 10:00 AM - Advances in Thin Wafer Debonding and Ultrathin 28-nm FinFET Substrate Transfer
Alain Phommahaxay, Anne Jourdain, Fabrice Fondjo and Jong-Hoon Kim – Georgia Institute of Technology

### 5. 10:25 AM - Thermally Reversible and Crosslinked Polyurethane based on Diels-Alder Alder Chemistry for Ultrathin Wafer Temporary Bonding at Low-Temperature Jinhui Li, Qiang Liu, Guoping Zhang, and Yong Sun – Shenzhen Institutes of Advanced Technology; Chingping Wong – Chinese University of Hong Kong

### 6. 10:50 AM - Synchrotron X-ray Microdiffraction Investigation of Scaling Effects on Plasticity and the Correlation to TSV Extrusion
Laura Spinella, Jang-hi Im, and Paul Ho – University of Texas, Austin; Tengfei Jiang – University of Central Florida

### 7. 11:15 AM - Development of High-Frequency Device using Glass or Fused Silica with 3D Integration
Yochiro Sato, Kohei Horiiuchi, and Motoshi Ono – Asahi Glass

## Session 17: Materials and Processes for Flexible and Wearable Devices

**Committee:** Emerging Technologies  
**Session Co-Chairs:**  
C. S. Premachandran – GLOBALFOUNDRIES  
Tel: +1-518-305-7317  
Email: premachandran.cs@globalfoundries.com  
Ankur Agrawal – Intel Corporation  
Tel: +1-480-516-2599  
Email: ankur.agrawal@intel.com

### 1. 8:00 AM - Nanoparticle Based Printed Sensors on Paper for Detecting Chemical and Biological Species
Jack Lombardi, Mark Poilus, Ning Kang, Jin Yan, Jing Li, Wei Zhao, Shuyan Shan, Jin Luo, and Chuan-Jian Zhong – Binghamton University; Benjamin Hisao – Stony Brook University

### 2. 8:25 AM - Phototriggerable Transient Electronics: Materials and Concepts
Oluwadamilola Phillips, Jared Schwartz, Anthony Engler, Gerald Gourdin, and Paul Kohl – Georgia Institute of Technology

### 3. 8:50 AM - Synthesis of a Soft Nanocomposite for Flexible, Wearable Bioelectronics
Fabricio Fonjdo and Jing-Hoon Kim – Washington State University; Michael Teller, Connor Howe, and Woon-Hong Yeo – Virginia Commonwealth University

### 4. 10:00 AM - BiCMOS Integrated Microfluidic Packaging by Wafer Bonding for Lab-on-Chip Applications
Mesut Inac – Technical University Berlin; Matthias Wietstruck, Alexander Görts, Barbaros Cetindogan, Canan Baristiran-Kaynak, Steffen Marschmeyer, Mirko Fraschke, Thomas Voss, Andreas Mai, and Mehmet Kaysin – IHP Microelectronics

### 5. 10:25 AM - Enhanced Thermal Performance Polyimide (PI) for Improved Flexible Electronic Application
Manuela Loeblein, Siu Hon Tsang, and Edwin Hang Yong Teo – Nanyang Technological University

### 6. 10:50 AM - Nanolaminated CoNiFe Cores with Dip-Coated Fluoroacrylic Polymer Interlamination Insulation: Fabrication, Electrical Characterization, and Performance Reliability
Minsoo Kim and Mark Allen – University of Pennsylvania; Joonchol Kim – Georgia Institute of Technology

### 7. 11:15 AM - Test Protocol for Assessment of Flexible Power Sources in Foldable Wearable Electronics Under Stresses of Daily Motion During Operation
Pradeep Lall and Hao Zhang – Auburn University

## Session 18: Warpage, Electromigration and Mechanical Characterization

**Committee:** Thermal/Mechanical Simulation & Characterization  
**Session Co-Chairs:**  
Xuejun Fan – Lamar University  
Tel: +1-409-880-7792  
Email: xuejun.fan@lamar.edu  
Jiantao Zheng – Qualcomm Technologies, Inc.  
Tel: +1-858-658-5738  
Email: jiantaaz@qti.qualcomm.com

### 1. 8:00 AM - Model for Interaction of EMC Formulation with the High Current Reliability of Cu-Al Wirebonds Operating in Harsh Environments
Pradeep Lall, Shantanu Deshpande, and Yihua Luo – Auburn University; Lui Nguyen – Texas Instruments, Inc.

### 2. 8:25 AM - Fan-Out Packages with High-Temperature Mold Compounds
Shreyas Dwarkanath, P. Markonduya Raj, Scott McCann, Jose Soler, Vanessa Smet, Rao Tummala, and Suresh Staranam – Georgia Institute of Technology

### 3. 8:50 AM - Non-Linear Viscoelastic Modeling of Epoxy Based Molding Compound for Large Deformations Encountered in Power Modules
Przemyslaw Gronola – Robert Bosch GmbH; Hyun-Seop Lee and Bongzai Han – University of Maryland

### 4. 10:00 AM - Warpage Modeling and Characterization of the Viscoelastic Relaxation for Cured Molding Process in Fan-Out Packages

### 5. 10:25 AM - Wafer Form Warpage Characterization Based on Composite Factors Including Pavitation Films, Re-Distribution Layers, Epoxy Molding Compound Utilized in Innovative Fan-Out Package

### 6. 10:50 AM - Co-Design for Low Warpage and High Reliability in Advanced Package with TSV-Free Interposer (TFI)
Fayng Che, Masaya Kawano, M. Z. Ding, Yong Han, and S. Bhattacharya – Institute of Microelectronics, A*STAR

### 7. 11:15 AM - Finite Elements for Electromigration Analysis
Bena Antonova and David Looman – Ansys, Inc.

**Refreshment Break: 9:15-10:00 a.m.**
# Program Sessions: Thursday, June 1, 1:30-5:10 p.m.

<table>
<thead>
<tr>
<th>Session 19: Recent Advances in FOWLP Technology</th>
<th>Session 20: MEMS and Sensor Technologies</th>
<th>Session 21: 3D Cu-Cu and Micro Bump Bonding Technologies</th>
</tr>
</thead>
<tbody>
<tr>
<td>Committee: Materials &amp; Processing</td>
<td>Committee: Advanced Packaging</td>
<td>Committee: Interconnections</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Session Co-Chairs:</td>
<td>Session Co-Chairs:</td>
<td>Session Co-Chairs:</td>
</tr>
<tr>
<td>Praveen Pandijairao – Johnson &amp; Johnson</td>
<td>Joseph W. Soucy – Draper Laboratory</td>
<td>Katsuyski Sakuma – IBM Corporation</td>
</tr>
<tr>
<td>Tel: +1-904-443-1691</td>
<td>Tel: +1-617-258-2953</td>
<td>Tel: +1-914-945-2080</td>
</tr>
<tr>
<td></td>
<td>Email: <a href="mailto:jsoucy@draper.com">jsoucy@draper.com</a></td>
<td>Email: <a href="mailto:ksakuma@us.ibm.com">ksakuma@us.ibm.com</a></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ho-Young Son – SK Hynix</td>
</tr>
<tr>
<td>Yi Li – Intel Corporation</td>
<td></td>
<td>Tel: +82-31-630-2858</td>
</tr>
<tr>
<td>Tel: +1-480-554-1657</td>
<td></td>
<td>Email: <a href="mailto:hoyoung.son@sk.com">hoyoung.son@sk.com</a></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1. 1:30 PM - Innovative Excimer Laser Dual</td>
<td>1. 1:30 PM - Fabrication of 3D Hybrid</td>
<td>1. 1:30 PM - Morphology Study of Bimodal-</td>
</tr>
<tr>
<td>Damascence Process for Ultra-Fine Line Multi-</td>
<td>Pixel Detector Modules based on TSV</td>
<td>Particle-Based All-Copper Interconnects</td>
</tr>
<tr>
<td>Layer Routing with 10um Pitch Micro-Vias for</td>
<td>Processing and Advanced Flip Chip</td>
<td>Formed at Low Sintering Temperature</td>
</tr>
<tr>
<td>Wafer-Level and Panel-Level Packaging</td>
<td>Assembly of Thin Read Out Chips</td>
<td>Luca Del Carro, Jonas Zuercher, and Thomas</td>
</tr>
<tr>
<td>Markus Woehrmann, Robert Gemhardt, Karm Hauck,</td>
<td></td>
<td>Brunswieler – IBM Corporation; Tom Wildsmith –</td>
</tr>
<tr>
<td>and Michael Toepfer – Fraunhofer IZM; Habib</td>
<td></td>
<td>Intrinsicq Materials; Gustavo Ramos – Atotech</td>
</tr>
<tr>
<td>Hichri and Markus Arend – Suss MicroTec;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Klaus-Dieter Lang – Technical University</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Berlin</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2. 1:55 PM - Forming a Vertical Interconnect</td>
<td>2. 1:55 PM - A Novel Technology for</td>
<td>2. 1:55 PM - Enabling Chip-To-Package Cu-Cu</td>
</tr>
<tr>
<td>Structure using Dry Film Processing for Fan-</td>
<td>Creating Sensors and Actuators in</td>
<td>Interconnections: Design of Engineered Bonding</td>
</tr>
<tr>
<td>Out Wafer Level Packaging</td>
<td>Processor Modules</td>
<td>Interfaces for Improved Manufacturability and</td>
</tr>
<tr>
<td>Yew Wing Leong, Hsiang-Yao Hsiao, David</td>
<td></td>
<td>Low-Temperature Bonding</td>
</tr>
<tr>
<td>Soon Wee Ho, Boon Long Lau, and Huamao Lin</td>
<td></td>
<td>Nind Shawane, Kathay Mohan, Antonia Antoniou, Puluurtha</td>
</tr>
<tr>
<td>– Institute of Microelectronics, A*STAR</td>
<td></td>
<td>Raj Markondy, Vanessa Smet, and Rau Tummala – Georgia</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Institute of Technology; Gustavo Ramos, Amid Kilar, and</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Robin Taylor – Atotech; Frank Wei – Disco Corporation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3. 2:20 PM - Embedded Trace RDL at 2-5um</td>
<td>3. 2:20 PM - Stress Compensating MEMS</td>
<td>3. 2:20 PM - Low-Temperature and Low-Pressure Cu-Cu</td>
</tr>
<tr>
<td>Width and Space by Excimer Laser, Cu Filling</td>
<td>Sensor Assembly</td>
<td>Bonding by Pure Nanosolder Paste for Wafer-Level</td>
</tr>
<tr>
<td>and Surface Planarization for 20-40um Pitch</td>
<td></td>
<td>Packaging</td>
</tr>
<tr>
<td>Interposers</td>
<td></td>
<td>Junjie Li, Tielin Shi, Xing Yu, Chaoxiang Cheng, Jinhu</td>
</tr>
<tr>
<td>Habib Hicht, Markus Arend, and Lee Seongluk</td>
<td></td>
<td>Fan, Guanglan Liao, and Zizong Tang – Huazong</td>
</tr>
<tr>
<td>– Suss MicroTec; Ruo Tummala and Venky</td>
<td></td>
<td>University of Science and Technology</td>
</tr>
<tr>
<td>Sundaram – Georgia Institute of Technology;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frank; Wei, Ye Chen, and Cody Lee –</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Disco; Ogner Dimov, Deepak Arora, and Sarjay</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Malik – Fujifilm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4. 3:30 PM - Temporary Bonding and</td>
<td>4. 3:30 PM - 3D Monolithic Metal Orifice</td>
<td>4. 3:30 PM - Dual Damascence Compatible, Copper Rich</td>
</tr>
<tr>
<td>Debonding Technologies for Fan-Out Wafer</td>
<td>Plating for Low-Cost MEMS Packaging</td>
<td>Alloy Based Surface Passivation Mechanism for</td>
</tr>
<tr>
<td>Level Packaging</td>
<td></td>
<td>Achieving Cu-Cu Bonding at 150°C for 3D IC Integration</td>
</tr>
<tr>
<td>Qi Wu, Xiao Liu, Kuo Han, Dongshun Bai, and</td>
<td></td>
<td>Asisa Kumar Panigrahi, Tamal Ghosh, Siva Rama</td>
</tr>
<tr>
<td>Tony Flaim – Brewer Science</td>
<td></td>
<td>Krishna Vanjari, and Shiv Govind Singh – Indian</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Institute of Technology, Hyderabad</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5. 3:55 PM - Development and Evaluation of</td>
<td>5. 3:55 PM - A Phase Sensitive</td>
<td>5. 3:55 PM - Thermal and Electrical</td>
</tr>
<tr>
<td>Carrier Glass Substrate for Fan-Out WLP/</td>
<td>Measurement Technique for Fast Recovery</td>
<td>Performance of Direct Bond Interconnect</td>
</tr>
<tr>
<td>PLP Process</td>
<td>of Graphene FET Gas Sensors</td>
<td>Technology for 1.5D and 3D Integrated</td>
</tr>
<tr>
<td>Kazutaka Hayashi, Shigeki Sawamura, Yu</td>
<td></td>
<td>Circuits</td>
</tr>
<tr>
<td>Harawa, Shuhei Nomura, and Jun Endo – Asahi</td>
<td></td>
<td>Akash Agrawal, Shouwu Huang, Guilian Gao, Liang</td>
</tr>
<tr>
<td>Glass Co.; Naoya Suzuki and Masaaki</td>
<td></td>
<td>Wang, and Laura Mrkanin – Insyenas Corporation</td>
</tr>
<tr>
<td>Takekoshi – Hitachi Chemical</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6. 4:20 PM - Warpage Suppression During</td>
<td>6. 4:20 PM - Comparison of Packaging</td>
<td>6. 4:20 PM - Electrical Performance of</td>
</tr>
<tr>
<td>FOWLP Fabrication Process</td>
<td>Concepts for High-Temperature Pressure</td>
<td>High-Density 10 µm Diameter 20 µm Pitch Cu-Pillar</td>
</tr>
<tr>
<td>Kesiuke Nishido, Yuhei Okada, Naoya Suzuki,</td>
<td>Sensors at 500°C</td>
<td>with Chip to Wafer Assembly</td>
</tr>
<tr>
<td>and Toshihisa Nonaka – Hitachi Chemical</td>
<td></td>
<td>Lucile Arnaud, Arnaud Garnier, Rémi Fanniante, Alan</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Toffoli, Stéphane Moreau, Franck Bana, Stéphane</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Moreau, and Séverine Chéramy – CEA-Leti</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7. 4:45 PM - Impact of Process Control on</td>
<td>7. 4:45 PM - High Vacuum and High</td>
<td>7. 4:45 PM - Morphological Evolution</td>
</tr>
<tr>
<td>UBM/RDL Contact Resistance on Next-</td>
<td>Robustness Al-Ge Bonding for Wafer</td>
<td>Affected by Surface Diffusion and Reaction-</td>
</tr>
<tr>
<td>Generation Fan-Out Devices</td>
<td>Level Chip Scale Packaging of MEMS</td>
<td>Induced Volume Shrinkage in Micro Joints</td>
</tr>
<tr>
<td>Patrik Carazzeto, Frantisek Balon, Mike</td>
<td>Sensors</td>
<td>Hong-Wei Yang and C. Robert Kao – National</td>
</tr>
<tr>
<td>Hoffmann, Juergen Weichert, Andreas Erhart,</td>
<td></td>
<td>Taiwan University</td>
</tr>
<tr>
<td>and Ewald Strolz – Evatec; Kay Vieheiger –</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fraunhofer IZM.ASSID</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Refreshment Break: 2:45-3:30 p.m.**
Session 22: Solder Joint & Interconnect Reliability, Characterization

<table>
<thead>
<tr>
<th>Committee: Thermal/Mechanical Simulation &amp; Characterization and Modeling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Session Co-Chairs:</td>
</tr>
<tr>
<td>Yong Liu – ON Semiconductor</td>
</tr>
<tr>
<td>Tel: +1-207-761-3155</td>
</tr>
<tr>
<td>Email: <a href="mailto:Yong.Liu@onsemi.com">Yong.Liu@onsemi.com</a></td>
</tr>
<tr>
<td>Erkan Oterkus – University of Strathclyde</td>
</tr>
<tr>
<td>Tel: +44 (0)141 548 3876</td>
</tr>
<tr>
<td>Email: <a href="mailto:erkan.oterkus@strath.ac.uk">erkan.oterkus@strath.ac.uk</a></td>
</tr>
</tbody>
</table>

1. 1:30 PM - Peridynamic Solution of Wetness Equation with Time-Dependent Saturated Concentration in ANSYS Framework
   Enologan Madenci and Cagan Duyaroglu – University of Arizona; Selda Oterkus and Erkan Oterkus – University of Strathclyde

2. 1:55 PM - A Modified Acceleration Factor Empirical Equation for BGA Type Package
   Min-Hsuan Hsu and Kuo-Ning Chiang – National Tsing Hua University; Chang-Chun Lee – National Chung Hsing University

3. 2:20 PM - Effect of Mean Temperature on the Evolution of Strain-Amplitude in SAC Ball-Grid Arrays During Operation Under Thermal Aging and Temperature Excursions
   Pradeep Lall, Kaz Mirza, and Jeff Suhling – Auburn University; David Locker – U.S. Army Aviation & Missile Research Development & Engineering Center

Refreshment Break: 2:45-3:30 p.m.

4. 3:30 PM - Development and Characterization of Dual Side Molding SIP Module Technology


6. 4:20 PM - Anisotropic and Multiscale Constitutive Framework for the Reliability of Microscale Interconnects Based on Damage Mechanics
   Zhengfang Qian – Shenzhen University

7. 4:45 PM - SACQ Solder Board Level Reliability Evaluation and Life Prediction Model for Wafer-Level Packages
   Wei Lin, Quan Pham, Bora Bora Baloglu, and Michael Johnson – Amkor Technology

Program Sessions: Thursday, June 1, 1:30-5:10 p.m.
**Program Sessions: Friday, June 2, 8:00-11:40 a.m.**

**Session 25: Characterization and Reliability of Fan-Out & WLP**
Committee: Applied Reliability

**Session 26: 3D Integration Processing and Reliability**
Committee: Advanced Packaging

**Session 27: Advances in Thermal Compression and Wirebonding**
Committee: Interconnections

---

**Session Co-Chairs:**
Lakshmi N. Ramanathan – Microsoft Corporation  
Tel: +1-425-421-3838  
Email: laranama@microsoft.com

Toni Mattila – Aalto University  
Tel: +358-405009909  
Email: toni.mattila@aalto.fi

---

**1. 8:00 AM - Paradoxical Role of Sulphur in Molding Compounds: Influence on High Temperature Reliability of Cu-Al Wirebond Interconnects**

**Session Co-Chairs:**
Rozalia Beica – Dow Electronic Materials  
Tel: +1-508-787-4691  
Email: rgbeica@dow.com

Dean Malta – Micro Advanced Interconnect Technology  
Tel: +1-919-248-8405  
Email: Dean.Malta@micross.com

---

**1. 8:00 AM - Fine Pitch Die-to-Si Interconnect Fabric (Si-IF) Interconnects using Thermal Compression Bonding**
Adeel Ahmad Bajwa, SvatChandra Jangam, Saptadeep Pal, Niteesh Marathe, Mark Goosney, Takafumi Fukushima, and Subramanian Iyer – University of California, Los Angeles

**Session Co-Chairs:**
Matthew Yao – GE Energy Management  
Tel: +1-412-963-3244  
Email: matthew.yao@ge.com

William Chen – Advanced Semiconductor Engineering, Inc.  
Tel: +1-408-250-4290  
Email: william.chen@aseus.com

---

**2. 8:25 AM - Mechanistic Investigation and Prevention of Al Bond Pad Corrosion in Cu Wire Bonded Device Assembly**
Oliver Chyan, Nick Ross, Alex Lambert, Seare Berhe, and Muthappan Asokan – University of North Texas; Mahmoud Chowdhury, Shawn O’Connor, and Luu Nguyen – Texas Instruments, Inc.

**Session 3: 8:50 AM - Use Condition Risk Assessment for Moisture-Related Failures**
Min Pei, Sibaish Mulkerjee, Nitin Uppal, and Milena Vuposevic – Intel Corporation

**Session 4: 10:00 AM - Drop Impact Reliability Test and Failure Analysis for Large Size High-Density FOWLP Package on Package**
ZhaoHui Chen – Institute of Microelectronics, A*STAR

**Session 5: 10:25 AM - The Comparative Study to Enhance Board Level Reliability Performance of Wafer Level Package at 0.25 mm Pitch Using Micro-Ball Drop and Electroplated Solder Technology**
Kuei Hisao Kuo, Yi Si Ding, Chui Feng Weng, Feng Lung Chen, Katch Wan, Chun Sheng Ho, and Rick Lee – Siliconware Precision Industries Co., Ltd.

**Session 6: 10:50 AM - Quality and Reliability Assessment of Cu Pillar Bumps for Fine Pitch Applications**
Othmane Jerhaoui, Stephane Moreau, David Bouchu, Gilles Romero, Denis Marisell, Thierry Mourier, and Arnaud Garnier – CEA-Leti

**Session 7: 11:15 AM - Effect of Prolonged Storage up to 1-Year on the High Strain Rate Properties of SAC Lead-Free Alloys at Operating Temperatures up to 200°C**
Pradeep Laithy, Pradeep Lal, Xi Zhang, Vikas Yadav, and Jeff Suhling – Auburn University; David Locker – U.S. Army Aviation & Missile Research Development & Engineering Center

**Session 8: 11:40 AM - Board Level Reliability Optimization for 3D IC Packages with Extra Large Interposer**
Laurene Yip, Ganesh Harinaran, Raghu Chaware, Inderjit Singh, and Tom Lee – Xilinx Corporation

**Session 9: 12:15 PM - Advances in Wire Bonding Technology for 3D Die Stacking and Fan-Out Wafer Level Packages**
Ivy Qin, Oranna Yauw, Gary Schulze, Aashish Shah, Bob Chylak, and Nelson Wong – Kulicke and Soffa

**Session Co-Chairs:**
Bob Chylak, and Nelson Wong – Kulicke and Soffa

---

**Refreshment Break: 9:15-10:00 a.m.**

**Session 10: 10:00 AM - Thermal Bond Reliability of High-Reliability New Palladium-Coated Copper Wire**
Motoki Eto, Teruo Haibara, Ryo Oishi, and Takashi Yamada – Nippon Micrometall; Tomohiro Uno – Nippon Steel & Sumitomo Metal

**Session 11: 10:25 AM - Correlation Study of Pd Metallurgical Distributions and RF Characteristics of Pd Coated/Doped Ag-alloy Wire Bonds**
Yi-Jung Sung and Lih-Tyng Hwang – National Sun Yat-Sen University; Chang-Yi Feng – NXP Semiconductor

**Session 12: 10:50 AM - Advances in Wire Bonding Technology for 3D Integration Processing and Wirebonding**

---

**Session 13: 11:15 AM - Development of High-Temperature Resistant Packaging of SiC Power Module for Automobile Application**
Kohki Tatsumi, Tornado Nonaka, Kazuhito Kamei, and Masakazu Inagaki – Waseda University; Akihiro Imakire and Masayuki Hikita – Kyushu Institute of Technology; Rikiya Kamimura – FAIS; Nobuaki Sato, Takafumi Fukushima, and Subramanian Iyer – University of California, Los Angeles

**Session Co-Chairs:**
Matthew Yao – GE Energy Management  
Tel: +1-412-963-3244  
Email: matthew.yao@ge.com

William Chen – Advanced Semiconductor Engineering, Inc.  
Tel: +1-408-250-4290  
Email: william.chen@aseus.com
1. 8:00 AM – High-Performance Insulating Adhesive Film for High-Frequency Applications
Junya Sato, Shin Teraki, Masashi Yoshida, and Hisao Kondo – NAMICS Corporation

2. 8:25 AM – Epoxy/Cyanate Ester Blend Material for Molding Compounds in High-Temperature Operations
Cha-Chi Tuan, Fan Wu, Kyoung-Sik Moon, Raj Pulugurtha, Ching-Ping Wong, and Rao Tummala – Georgia Institute of Technology

3. 8:50 AM – High Thermal Conductivity Mold Compounds for Advanced Packaging Applications
Makoto Shibuya and Luu Nguyen – Texas Instruments, Inc.

4. 10:00 AM – Enhanced Thermal Conductivity of the Underfill Materials using Insulated Core/Shell Filler Particles for High-Performance Flip Chip Applications
Tae-Ryong Kim, Kisu Joo, and Se Young Jeong – Nihum Inc.; Boo Tak Lim and Boong Ju Lee – National Nanofab Center; Sung Soon Choi – Korea Electronics Technology Institute; Myung Jin Yim – Intel Corporation; Euijoon Yoon – Seoul National University

5. 10:25 AM – High Thermal Performance Package with Anisotropic Thermal Conductive Material
Ian Hu, Janea Ho, Penny Yang, and C. P. Hung – Advanced Semiconductor Engineering, Inc.

6. 10:50 AM – Reduction of Outgases from Pre-Applied Underfill Materials by Optimizing the Combination of Base Resin and Flux Compound
Kohei Higashiguchi, Takenori Takiguchi, Masashi Okaniwa, Katsumoto Ihara, Tsuyoshi Kida, Shu Yoshida, and Toyoi Oshima – Mitsubishi Gas Chemical

7. 11:15 AM – Study of Capillary Underfill Filler Separation in Advanced Flip Chip Packages
Marie-Claude Paquet – IBM Corporation; David Danovitch – Université de Sherbrooke

8. 8:00 AM – Innovative Advances in Copper Electroplating for IC Substrate Manufacturing
Kousik Ganesh, Yang Sun, Chandreshkhar Pendyala, Thomas Heaton, Radek Chalupa, Marcel Wall, Sudhasatwa Nad, Andrew Wentzel, and Rahul Maneppalli – Intel Corporation; Amaneh Tasooji – Arizona State University

2. 8:25 AM – Reflow Warpage Induced Interconnect Gaps Between Package and PCB and PoP Top and Bottom Packages
Kaiqang Peng, Wei Xu, Zhenkai Qin, Lei Feng, Lin Lin, and Wei Hu Koh – Huawei Technologies

3. 8:50 AM – Warpage Tuning Study for Multi-Chip Last Fan-Out Wafer Level Package
Hung-Tuan Li, Allen Chen, Sam Peng, George Pan, and Stephen Chen – Siliconware Precision Industries Co., Ltd.

4. 10:00 AM – Warpage Characterization of Glass Interposer Package Development
Mengkai Shih, Charles Hsu, Yungshun Chang, Karenyu Chen, and Ian Hu – Advanced Semiconductor Engineering, Inc.

5. 10:25 AM – The Influence of Resin Coverage on Reliability for Solder Joints Formed by One-Pass Reflow using Resin Reinforced Low-Temperature Solder Paste
Atsushi Yamaguchi, Yasuo Fukuhara, Andy Behr, Naomichi Ohashi, Yasuhiro Suzuki, and Hirohisa Hino – Panasonic Corporation

6. 10:50 AM – Analysis of System-Level Reliability of Single-Chip Glass BGA Packages with Advanced Solder and Polymer Collars
Vidy Jyaram, Scott McCann, Bhupender Singh, Pulugurtha Markondeya Raj, Ting-Chia Huang, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology; Hiro Matuura and Yutaka Takagi – NTK/NOK

7. 11:15 AM – A Comprehensive Study on Stress and Warpage by Design, Simulation and Fabrication of RDL-First Panel Level Fan-Out Technology for Advanced Package
Puru Lin, Cheng-Ta Ko, and Yu-Hua Chen – Unimicron

8. 8:00 AM – Next Generation High-Q Compact Size IPD Diplexer for RF Front End SIP
Sheng-Chi Hsieh, Pao-Nan Lee, Chen-Chao Wang, Teck Chong Lee, and Hsu-Chang Shih – Advanced Semiconductor Engineering, Inc.

2. 8:25 AM – Self-Actuating 3D Printed Packaging for Deployable Antennas
Ryan Bahr and Manos Tzentiris – Georgia Institute of Technology

3. 8:50 AM – A Simple and Efficient RF Technique for the TSV Characterization
Xiao Sun, Stefaan Van Huylenbroeck, Geert Van der Plas, and Eric Beyne – IMEC; Cesar Roda Neve – M3 Systems

4. 10:00 AM – Smallest Form Factor GPS for Mobile Devices
Ebrahim Andideh, Chuck Carpenter, Jason Steigliner, Mike Yore, James Tung, Lynda Koerber, David Schnauffer, Bharati Ingle, Suwanna Jittinorasett, and Otto Berger – Qorvo, Inc.

5. 10:25 AM – Transparent Antennas for Wireless Systems based on Patterned Indium Tin Oxide and Thin Flexible Glass
Mark Pollis, Yi-Lin Sung, Jack Lombard, Robert Malay, and Charles Westgate – Binghamton University; Ming-Huang Huang, Sean Garner, Scott Pollard, and Colin Daley – Corning, Inc.

6. 10:50 AM – Designs and Characterizations of RF 3D Module Based on Si Interposers
Kwang-Seong Choi, Leeseul Jeong, Seok Hwan Moon, Yong-Sung Eom, Hyun-Cheol Bae, and Jin Ho Lee – Electronic and Telecommunication Research Institute

7. 11:15 AM – An Electronic Nose for Wireless Sensing of Volatiles by Capillary Condensation
Saranaj Karuppaswami, Armanpreet Kaur, and Premjeet Chahal – Michigan State University; Nophadon Wivatcharangoses – Mongkut’s University of Technology
<table>
<thead>
<tr>
<th>Session 31: Auto Electronics Packaging and Power Modules</th>
<th>Session 32: Reliability Challenges in 2.5D/3D Interconnect</th>
<th>Session 33: Advanced Bonding and Soldering Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Committee:</strong> Advanced Packaging</td>
<td><strong>Committees:</strong> Interconnections joint with Applied Reliability</td>
<td><strong>Committee:</strong> Materials &amp; Processing</td>
</tr>
<tr>
<td>Tel: +1-508-229-7117 Email: <a href="mailto:jianweidong@dow.com">jianweidong@dow.com</a></td>
<td>Tel: +1-319-295-6687 Email: <a href="mailto:nathan.lower@rockwellcollins.com">nathan.lower@rockwellcollins.com</a></td>
<td>Tel: +1-573-201-8669 Email: <a href="mailto:kyess@brewerscience.com">kyess@brewerscience.com</a></td>
</tr>
<tr>
<td>Christophe Zinck – Advanced Semiconductor Engineering, Inc. Tel: +33-628566802 Email: <a href="mailto:Christophe.Zinck@aaseu.com">Christophe.Zinck@aaseu.com</a></td>
<td>Dongji Xie – NVIDIA Corporation Tel: +1-408-486-8630 Email: <a href="mailto:dongji@nvidia.com">dongji@nvidia.com</a></td>
<td>Qianwen Chen – IBM Corporation Tel: +1-914-945-1612 Email: <a href="mailto:chenq@us.ibm.com">chenq@us.ibm.com</a></td>
</tr>
</tbody>
</table>

1. 1:30 PM - Novel Polymer Substrate-Based 1.2 kV/40 A Double-Sided Intelligent Power Module
Xin Zhao, Bo Gao, and Douglas Hopkins – North Carolina State University

2. 1:55 PM - Advanced Packaging Need for Automotive Dashboard Application
Nokbul Islam, MC Hseh, and KyungOe Kim – STATS ChipPAC

3. 2:20 PM - Reliability of eWLB (embedded wafer level BGA) for Automotive Radar Applications
Daniel Yap, Kim Sing Wong, and Luc Pett – STMicroelectronics; Yaojian Lin – STATS ChipPAC

4. 3:30 PM - Remarkable Suppression of Local Stress in 3D IC by Manganese Nitride-Based Filler with Large Negative CTE
Hitoshi Kino, Takafumi Fukushima, and Tetsu Tanaka – Georgia Institute of Technology; Tomonori Ogawa – Asahi Glass

5. 3:55 PM - Electrical Characterization of CMP-Less Via-Last TSV under Reliability Stress Conditions
Mingbin Yu – Institute of Microelectronics, A*STAR

6. 4:20 PM - A Novel Failure Analysis Technique for Semiconductor Packaging by XeF2 Gas
Hongqiang Zhang, Frank Pompeo, and Tom Wassick – IBM Corporation

7. 4:45 PM - Strain Quantification of Microbumps at the Intermetallic Rich Zone
Huayan Wang, Yuling Niu, and Seungbae Park – Binghamton University

8. 4:45 PM - Ga Liquid Metal Embrittlement for Fine Pitch Interconnect Rework
Yolande Elodie Nguena Dongmo, David Danovitch, and Malak Kanso – University of Sherbrooke; Richard Langlois – IBM Corporation
**Program Sessions: Friday, June 2, 1:30-5:10 p.m.**

<table>
<thead>
<tr>
<th>Session 34: Waveguide Devices and Chip-to-Fiber Packaging</th>
<th>Session 35: Thermomechanical and Thermal Characterization</th>
<th>Session 36: Advances in Signal and Power Integrity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Committee: Optoelectronics</td>
<td>Committee: Thermal/Mechanical Simulation &amp; Characterization</td>
<td>Committee: High-Speed, Wireless &amp; Components</td>
</tr>
<tr>
<td>Session Co-Chairs:</td>
<td></td>
<td>Session Co-Chairs:</td>
</tr>
<tr>
<td>Ping Zhou – LDX Optronics, Inc.</td>
<td></td>
<td>Zhaoqing Chen – IBM Corporation</td>
</tr>
<tr>
<td>Tel: +1-865-981-8822</td>
<td></td>
<td>Tel: +1-845-435-5995</td>
</tr>
<tr>
<td>Email: <a href="mailto:pingzhou@ldxoptronics.com">pingzhou@ldxoptronics.com</a></td>
<td></td>
<td>Email: <a href="mailto:zhaoqing@us.ibm.com">zhaoqing@us.ibm.com</a></td>
</tr>
<tr>
<td>Hiren Thacker</td>
<td></td>
<td>Amit P. Agrawal – Keyssa Inc.</td>
</tr>
<tr>
<td>Tel: +1-619-940-7803</td>
<td></td>
<td>Tel: +1-408-666-8452</td>
</tr>
<tr>
<td>Email: <a href="mailto:hiren@tech301.com">hiren@tech301.com</a></td>
<td></td>
<td>Email: <a href="mailto:Ap_agrawal@yahoo.com">Ap_agrawal@yahoo.com</a></td>
</tr>
</tbody>
</table>

1. 1:30 PM - Design, Fabrication and Connectorization of High-Performance Multimode Glass Waveguides for Board-Level Optical Interconnects
   Lars Brusberg, Davide Fortunisi, Wei Jiang, Aramis Zakharian, Sergey Kuchinsky, Christian Feibig, Shenping Li, Andrey Kobyakov, and Alan Evans – Conning; Henning Schröder – Fraunhofer IZM

2. 1:55 PM - Axially Tapered Circular Core Polymer Optical Waveguides Enabling Highly Efficient Light Coupling
   Kenji Katori, Hoshikiko Toda, and Kazuki Yasuhara – Keio University

3. 2:20 PM - First Demonstration of Single-Mode Polymer Optical Waveguides with Circular Cores for Fiber-to-Waveguide Coupling in 3D Glass Photonic Interposer
   Rui Zhang, Bruce C Chou, Fuhan Liu, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Michael Gallagher and Corey O’Connor – Dow Chemical

4. 3:30 PM - Optical Coupling Techniques on Polymer Waveguides for Wafer and Board Level Integration
   Sebastian Lingen, Sujoy Charrana, Tobias Tiedje, Krzysztof Nieweglowski, Sebastian Kilge, Lukas Lorenz, Johann W. Barth, and Karlheinz Bock – Technical University Dresden

5. 3:55 PM - Position Dependence of Coupling Efficiency of Grating Coupler in Waveguide Cavity
   Shogo Ura, Kazuki Masaoka, Ryo Tsujimoto, and Junichi Inoue – Kyoto Institute of Technology; Kenji Kintaka – National Institute of Advanced Industrial Science and Technology

6. 4:20 PM - Efficient, Easy-to-Use, Planar Fiber-to-Chip Coupling Process with Angle-Polished Fibers
   Djom Kamick, Nils Baudtsch, Lars Eisenblätter, Thomas Kühner, Marc Schneider, and Marc Weber – Karlsruhe Institute of Technology (KIT)

7. 4:45 PM - Novel, High-Throughput Fiber-to-Shell Assembly Employing Only Off-the-Shelf Components
   Nicolas Böyer, Stephan Martel, Swetha Kamlapurkar, Sebastian Engelmann, Paul Fortier, and Tymon Barwicz – IBM Corporation; Alexander Janta-Polczynski – ICM; Jean-Francois Morissette – Université de Sherbrooke

8. 1:30 PM - The Combined Effect of Mechanical Package Stress and Humidity on Chip Corrosion Probability
   Georg Lorenz and Michel Simon-Najasek – Fraunhofer IMWS; Achim Lindner – TDK-Micronas GmbH

9. 1:55 PM - High Voltage and High Temperature Capacitors for Next-Generation Power Modules in Electric Vehicles

10. 2:20 PM - Package-Level Si Micro-Fluid Cooler with Enhanced Jet Array for High-Performance 3D Systems
    Yong Han, Boon Long Lau, and Gongyue Tang – Institute of Microelectronics, A*STAR; Seow Meng Low and Jason Goh – BeCe Pte. Ltd.

11. 2:45-3:30 p.m. Refreshment Break

12. 3:30 PM - Signal and Power Integrity Analysis of High-Speed Links with Sip Interposer
    Wendem Beyene, Nitin Jallia, Yeon-Chang Hahn, Ravi Kollipara, and Joohee Kim – Rambus, Inc.

13. 3:55 PM - Novel Parallel Resonance Peak Measurement and Modeling Technique for 2-T and 3-T MLCC Capacitors for PDN Application
    Larry Smith, Javid Mohamed, Jaemin Shin, and Tim Michalka – Qualcomm Technologies, Inc.

14. 4:20 PM - Research on Ionic Wind and Its Cooling Ability Based on Finite Element Method
    Chunlin Xu and Shannan Zhan – Huazhong University of Science & Technology; Hui Zheng and Sheng Liu – Wuhu University

15. 4:45 PM - System-Driven On-chip SI/PI Solutions in Ultra-Low Cost Non-Term 1600+ Mbps LPDDR3/DDR3/DDR4
    Ching-Hwa Wu, Hung-Chuan Chen, Yingmin Liao, and Shang-Ping Chen – MediaTek

16. 1:30 PM - Active and Passive Techniques for Noise Sensitive Circuits in Integrated Voltage Regulator based Microprocessor Power Delivery
    Amit Jain, Sameer Shekhar, and Yan Li – Intel Corporation

17. 1:55 PM - Mechanical Characterization of Anodic Bonding using Chevron-Shaped Microchannel
    David Woodrum and Suresh Staraman – Georgia Institute of Technology

18. 2:20 PM - Package and Printed Circuit Board Design of a 19.2 Gb/s Data Link for High-Performance Computing
    Sungun Chun, Jose Hesae, Junyao Tang, Jean Audet, Dale Becker, Daniel Drees, Glen Wiedemer; Megan Nguyen, Lloyd Walls, Francesco Preda, and Daniel Douret – IBM Corporation

19. 3:30 PM - A Unified and Versatile Model Study for Moisture Diffusion
    Liangbiao Chen – Lamar University

20. 3:55 PM - Microstructure Simulation and Thermo-Mechanical Behavior Analysis of Copper-Filled Through Silicon Vias Using Coupled Phase Field and Finite Element Methods
    Shuai-Bao Liang, Chang-Bo Ke, Han Jiang, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology

21. 4:20 PM - Measurement and Modeling Technique for Through-Silicon Vias
    Joungho Kim – Korea Advanced Institute of Science & Technology; Heegon Kim – MST

22. 4:45 PM - System-Driven On-chip SI/PI Solutions in Ultra-Low Cost Non-Term 1600+ Mbps LPDDR3/DDR3/DDR4
    Ching-Hwa Wu, Hung-Chuan Chen, Yingmin Liao, and Shang-Ping Chen – MediaTek

23. 1:30 PM - The Combined Effect of Mechanical Package Stress and Humidity on Chip Corrosion Probability
    Georg Lorenz and Michel Simon-Najasek – Fraunhofer IMWS; Achim Lindner – TDK-Micronas GmbH

24. 1:55 PM - High Voltage and High Temperature Capacitors for Next-Generation Power Modules in Electric Vehicles

25. 2:20 PM - Package-Level Si Micro-Fluid Cooler with Enhanced Jet Array for High-Performance 3D Systems
    Yong Han, Boon Long Lau, and Gongyue Tang – Institute of Microelectronics, A*STAR; Seow Meng Low and Jason Goh – BeCe Pte. Ltd.

26. 2:45-3:30 p.m. Refreshment Break

27. 3:30 PM - Signal and Power Integrity Analysis of High-Speed Links with Sip Interposer
    Wendem Beyene, Nitin Jallia, Yeon-Chang Hahn, Ravi Kollipara, and Joohee Kim – Rambus, Inc.

28. 3:55 PM - Novel Parallel Resonance Peak Measurement and Modeling Technique for 2-T and 3-T MLCC Capacitors for PDN Application
    Larry Smith, Javid Mohamed, Jaemin Shin, and Tim Michalka – Qualcomm Technologies, Inc.

29. 4:20 PM - Research on Ionic Wind and Its Cooling Ability Based on Finite Element Method
    Chunlin Xu and Shannan Zhan – Huazhong University of Science & Technology; Hui Zheng and Sheng Liu – Wuhu University

30. 4:45 PM - System-Driven On-chip SI/PI Solutions in Ultra-Low Cost Non-Term 1600+ Mbps LPDDR3/DDR3/DDR4
    Ching-Hwa Wu, Hung-Chuan Chen, Yingmin Liao, and Shang-Ping Chen – MediaTek
Interactive Presentations: Wednesday, May 31, 9:00 a.m. - 11:00 a.m. and 2:00 p.m. - 4:00 p.m.

Wednesday, May 31, 2017
Session 37: Interactive Presentations 1
9:00 a.m. - 11:00 a.m.

Committee: Interactive Presentations
Session Co-Chairs:
Rao Bonda
Amkor Technology
Tel: +1-480-786-7749
Email: rao.bonda@amkor.com
John Hunt
Advanced Semiconductor Engineering, Inc.
Tel: +1-480-718-8011
Email: john.hunt@aseus.com
Deborah S. Patterson
Principal, Patterson Group
Tel: +1-480-703-5683
Email: deborah@patterson-group.com
Andy Tseng
JSR Micro
Tel: +1-408-472-7345
Email: atseng@jsrmicro.com

Fine Pitch Cu Pillar with Bond on Lead (BOL) Assembly Challenges for Low-Cost and High-Performance FCBGA Package
Nokibul Islam, Vinyak Pandey, and KyungOe Kim – STATS ChipPAC

Compression Molding Encapsulants for Wafer-Level Embedded Active Devices (TSV)
Ki Hyeok Kwon, Youonan Lee, Dong Hwan Lee, and Sang Kyun Kim – Samsung SDI; Kunis Ulee, Dong Kwan Kim, and Chul Woo Kim – Samsung Electronics

A Density Staggered Cantilever for Micron Length Gravity Probing
Qidong Wang – Institute of Microelectronics/Stanford University

Flip Chip Solder Joint Pad Optimizations for Connectivity SIP Applications
Quan Qi and Carlton Hanna – Intel Corporation

Scalability and Yield in Elastomer Stamp Micro-Transfer-Printing

High Transmittance Broadband THz Polarizer using 3D-IC Technologies
Nai-Chen Chi, Ting-Yang Yu, Hsin-Cheng Tsai, Chih-Wei Luo, and Kuan-Neng Chen – National Chiao Tung University; Shiang-Yu Wang – Academia Sinica

High Accuracy Thermal Compression Bonding Technology for Large-Sized Substrate
Noboru Asahi, Toshiyuki Jinda, Yoshioho Mizutani, Koichi Imai, Hikaru Tomita, Mikio Kawakami, Masafumi Senda, and Katsumi Terada – Toray Industries

Real-Time Tunable Color White LED Through Combination of Phosphor Patterns and Adaptive Liquid Lens
Hui Zhang – Wuhan University

Yield Comparison of Die-First Face-Down and Die-Last Fan-Out Wafer Level Packaging
Amy Lujan – SavanSys Solutions, LLC

Assembly Challenges for 75x75mm² Large Body FCBGA with Emerging High Thermal Interface Material (TIM)
Fletcher (Cheng-Piao) Tsung, Max (Chin Yü) Lu, Albert (Chang Yi) Lan, and Steward (Chn An) Pan – Siliconware Precision Industries Co., Ltd.

V-DOE Laser Full Cut Dicing of Thin Si IC Wafers
Jeroen van Borkulo, Paul Verburg, and Richard van der Stam – ASM Pacific Technologies

A New Method for 3D Microstructure Fabrication via Ionic Wind
Shangru Zhou, Guoliang Li, Hui Zheng, and Sheng Liu – Wuhan University

A Unique Temporary Bond Solution Based on a Thermoplastic Material Tacky at Room Temperature and Highly Thermally Resistant Application Extension from 3D-SIC to FOWLP
Alani Phommahaxay, Goedele Potoms, Julien Bertheau, Pieter Bex, Teng Wang, Fabrice Duval, Amrita Podpod, and Eric Beyne – IMEC; Atsushi Nakamura and Yoshitaka Kamochi – FUJIFILM

3D Printed Out-of-Plane Antennas for Microwave and Millimeter Wave Applications
Mehdi Iwaz, Mohd Ghazali, Saranraj Karuppuswami, Amanpreet Kaur, Jennifer Byford, Jonathan Frasch, James Lennon, and Premjeet Chahal – Michigan State University

Wednesday, May 31, 2017
Session 38: Interactive Presentations 2
2:00 p.m. - 4:00 p.m.

Committee: Interactive Presentations
Session Co-Chairs:
Nam Pham
IBM Corporation
Tel: +1-512-286-8011
Email: npham@us.ibm.com
Patrick Thompson
Texas Instruments, Inc.
Tel: +1-214-567-0660
Email: patrick.thompson@ti.com
Eric Beyne
IMEC
Tel: +32-16-281-261
Email: eric.beyne@imec.be
Richard Rao
MicroSemi
Tel: +1-805-914-2272
Email: Richard.rao@microsemi.com

Exploring Multi-Drop DDR4 Address Bus Design for 4GTS and Higher Speed Data
Nanju Na, Juan Wang, Sean Long, Changyi Su, Thomas To, Yong Wang, and Dima Klokov – Xilinx Corporation

Transfer Function Reconfigurable Cavity Bandpass Filter Embedded with Metallic Grid
Shang-Yu Hung, Guann-Pyng Li, Mark Bachman, Hsiang-Yu Chan, and Zhihao Zhang – University of California, Irvine

Signal Integrity Modelling in Inhomogeneous Waveguide/PCB of Arbitrary Shape Using Broadcast Green’s Function
Kung-Hau Ding – Air Force Research Laboratory; Tien-Hao Liao and Leung Tsang – University of Michigan

RF Characterization and Modeling of 10mm Fine-Pitch Cu-Pillar on a High-Density Silicon Interposer
HelèneJacquinet – CEA-Leti

A Novel Frequency-Modulated Power Delivery Network Design for DRAM Interface in Low-Cost WireBond Package
Sheng-Feng Lee, Chia-Yu Chan, and Shang-Pin Chen – MediatTek Corporation
Compact Thin-Film Broadband Millimeter-Wave Bandpass Filters on Low-Loss Glass Interposers using Evanescent Mode Eighth-Mode Substrate Integrated Waveguide Cavities
David Senior – Anaren Microwave; Seohee Hwangbo and Yong-Kyu Yoon – University of Florida; Aric Shorey – Coming; Jungkwon Kim – University of Kansas

New Wave Fan-Out Package Design and Electrical Analysis in Mobile Application
Tsun-Lung Hsieh, Po-Chih Pan, Chih-Yi Huang, Ming-Fong Jong, and Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.; Yuan-Hsi Chou – The University of Texas, Austin

Multi-Band Harmonic RF Tags for Barcode Applications in a Cluttered Environment
Saranraj Karuppuswami, Mohd Ifwat Mohd Ghazali, Anmapreet Kaur, and Premjeet Chahal – Michigan State University

TSV-Integrated High-Band AIN Based RF-MEMS Resonator for Mobile and Wireless Applications
Nan Wang, Yao Zhu, Chengliang Sun, Mingbin Yu, Geng Li Chua, Srinivas Merugu, Navab Singh, and Yuandong Gu – Institute of Microelectronics, A*Star

Equalization Enhancement Approaches for PAM4 Signaling for Next-Generation Speeds
Jiayi He, Nana Dikhaminjia, Mikhail Tsiklauri, and James Drewniak – Missouri University of S&T; Bhuvay Mutrny and Anur Chada – Dell, Inc.

Data Transfer Performance Analysis and Enhancement of Critical 3D Interconnects in a 3D SIP based on Communication Channel Modeling Methodology
Min Miao, Zhensong Li, and Xiaoyang Duan – Beijing Information Science and Technology University; Xiaole Cui and Yufeng Jin – Peking University

A Comprehensive Reliability Assessment of Electronic Packages with Digital Image Correlation Method
Yuling Niu, Jing Wang, and Seungbae Park – State University of New York at Binghamton; Van-Lai Pham – State University of New York, Binghamton

A New and Effective EMI Shield Method with Nanomagnetic Multilayered Film Composite
Ji-Hye Lee, Kyong Chul Bae, Yoonman Lee, Junghwa Kim, Dong Hwan Lee, and Sang Kyeun Kim – Samsung SDI

New Analytical Method for Assessing Thermo-Mechanical Stress-Induced Damage to WL CSP Solder Interconnects
Tae-Kyu Lee – Portland State University; Weidong Xie, Steven Peng, Cherif Guirguis, and Kola Akinade – Cisco Systems; Edward Ibe and Karl Loh – Zymet, Inc.

Real-Time Diagnosis of Wire Degradation based on Digital Signal Analysis
Jinwo Lee and Daeil Kwon – Ulsan National Institute of Science and Technology

FE Simulation of Joint-to-Joint Variation of Temperature during Thermo-Compression Bonding
Depaney Athia and Michael Mayer – University of Waterloo; Alineza Rezvani, Horst Claebourg, and Ivy Qin – Kulicke and Soffa

A Low-Cost and Compact 100G PAM-4 ROSA using TO-Can Package
Sae-Kyoung Kang, Je Hyun Lee, Joong Young Huh, and Joon Ki Lee – Electronics and Telecommunications Research Institute

Comparison and Consistency of On-PCB Microstrip Line Modeling by 3D Fullwave and 2D Quasi-Static Approaches for High-Speed Packaging System Signal Integrity Simulations
Zhaqing Chen – IBM Corporation

Development of Die Attachment Technology for Power IC Module by Inducing Indium into Sintered Nano-Silver Joint
Chun An Yang and C. Robert Kao – National Taiwan University; Hiroshi Nishikawa – Osaka University

Effect of Nickel-Coating Modified CNTs on the Dopant Dispersion and Performance of BGA Solder Joints
Huayan Hu and Yan-Cheong Chan – City University of Hong Kong; Xiao-Hu – Hisilicon Technologies; Fengshun Wu – Huazhong University of Science and Technology

Small Event Probability Analysis of Manufacturing Problems with Numerous Input Variables using Advanced Uncertainty Propagation Analysis
Hsiu-Ping Wei and Bongtae Han – University of Maryland

Alternative 3D Small Form Factor Methodology of System in Package for IoT and Wearable Devices Application
Mike Tsai, Albert Lan, Chi Liang Shih, Terence Huang, Ryan Chiu, S. L. Chung, J. Y. Chen, Frank Chu, Cheng Kai Chang, and Nicholas Kao – Siliconware Precision Industries Co., Ltd.

First Demonstration of Photoresist Cleaning for Fine Line RDL Yield Enhancement by an Innovative Ozone Treatment Process for Panel Fan-out and Interposers
Atul Gupta, Eric Snyder, Christiane Gottschalk, James Gunn, and Kevin Wenzel – MKS Instruments; Hao Lu, Yuya Suzuki, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology
**Interactive Presentations:** Thursday, June 1, 9:00 a.m. - 11:00 a.m. and 2:00 p.m. - 4:00 p.m.

**Assessing the Reliability of High-Temperature Solder Alternatives**
Maa Z. Kokash, Rajesh S. Sivasubramony, Jorge L. Then Cuevas, Angelo F. Zamudio, Thaer Alghoul, and Peter Borgesen – Binghamton University; Alfred A. Zinn, Randall M. Stoltenberg, Jerome Chang, Y. L. Tseng, and Dan Blass – Lockheed Martin

**High Performance Silver Alloy Bonding Wire for Memory Devices**
Tetsuya Oyamada, Tomohiro Uno, and Takashi Yamada – Nitto Denko; Sumitomo Metal; Daizo Oda – Nitto Micromet

**Discussions of a Methodology for Determining Void Errors in Wafer Bonding and 3D Structures**
Mark Plennmons and William Kerr – Evergreen Enhancement

**Development of Liquid, Granule, and Sheet Type Epoxy Molding Compounds For Fan-Out Wafer Level Package**
Kenichi Ueno, Kazuhiro Dohi, Kazuyoshi Muranaka, Akira Nakao, and Yuki Ishikawa – Sanyu Rec

**Low Pressure Solid-State Bonding using Silver Preforms for High Power Device Packaging**
Jiaqi Wu and Chin C. Lee – University of California, Irvine

**Fabrication, Characterization and Comparison of FR4-Compatible Composite Magnetic Materials for High-Efficiency Integrated Voltage Regulators with Embedded Magnetic Core Micro-Inductors**
Mohamed Bellarej, Sebastian Mueller, Anto Davis, Paul Kohl, and Madhavan Swaminathan – Georgia Institute of Technology; Yashuiko Mano – ibiden

**The Novel Failure Mechanism of the Polymer Ball Interconnected CBGA Under Board Level Thermal Mechanical Stress**
Jeffrey Lee and Cheng-Chih Chen – Integrated Service Technology, Inc.

**Development of Double Side Protection Process with Bump Support Film (BSF) and Backside Coating Tape for WLP**
Masanori Yamagishi, Keisuke Shinomiya, Tomotaka Morishita, Motoki Nozue, Akinori Sato, and Shinya Taku – LINTEC

**Selective Laser Melting as an Alternative for Production of High-Temperature Power Electronic Substrates**
Aarief Syed Khaja and Joerg Franke – Friedrich Alexander University

**Design of Miura Folding Based Micro-Supercapacitor Arrays with Higher Areal Densities as Foldable and Miniaturized Energy Storage Units**
Bo Song, Yun Chen, Kyoung-sik Moon, and C. P. Wong – Georgia Institute of Technology

**Assembly and Reliability Challenges for Next-Generation High-Thermal TIM Materials**
Chi-An Pan, Chi-Tung Yeh, Wei-Chun Qiu, Rong-Zheng Lin, Liang-Yih Huh, Kang-Toon Ng, C. F. Lin, C. Key Chung, Don-Son Jang, and C. S. Hsiao – Siliconware Precision Industries Co., Ltd.

**Low-Temperature Curable Polyimide Film Properties and WLP Reliability Performance with Various Curing Conditions**
Steven Chen; Katch Wan, Chen An Chang, and Rick Lee – Siliconware Precision Industries Co., Ltd.

**Effects of Polymer Rebond on Crack-Free Acrylic based SnBi58 ACFs (Anisotropic Conductive Films) Joints during a Thermal-Compression Bonding Method**
Shuye Zhang and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

**Thursday, June 1, 2017 Session 40: Interactive Presentations 4:00 p.m. - 4:00 p.m.**

**Committee: Interactive Presentations**
Session Co-Chairs: Ibrahim Guven

**Virginia Commonwealth University**
Tel: +1-804-827-3652
Email: iguven@vcu.edu

**Mark Poliks**
Binghamton University
Tel: +1-607-727-7104
Email: mpoliks@binghamton.edu

**Nancy Iwamoto**
Honeywell
Tel: +1-760-788-7109
Email: nancy.iwamoto@honeywell.com

**Jai Agrawal**
Purdue University
Tel: +1-408-772-6727
Email: jaipagrawal@gmail.com

**Pod Cratering Based Failure Criterion for the Life Prediction of Board-Level Cyclic Bending Test**
Qiming Zhang, Jeffery C. C. Lo, and Shi-Wei Ricky Lee – Hong Kong University of Science and Technology

**An Accurate Dynamic Thermal Model for Electronic Parts and its Applications in System-Level Thermal Simulations**
An-Yu Kuo, C. T. Kao, and Xin Ai – Cadence Design Systems; Vijay Pandian – Future Facilities

**Equivalent Thermal Conductivity Model Based Full-Scale Numerical Simulation for Thermal Management in Fan-Out Packages**
Ningyu Wang, Yudan Pi, Wei Wang, and Yufeng Jin – Peking University

**Experimental and Finite Element Study about the Influence of Stress on the Electromigration Life of Solder**
Fei Su, Zheng Zhang, Qingyi Liu, Xiaoxu Pan, and Qizhi Wang – Beijing University of Aeronautics and Astronautics

**A Bugle Test to Investigate Mechanical Properties of Thin Adhesive Layer**
Pei Chen, Jinglong Sun, Tian Pan, and Fei Qin – Beijing University of Technology

**Local Stress Analysis by Kossel Diffraction Applied on Flip Chip Structure**
Anne-Laure Lebady and Manuel Fendler – CEA-Leti; Raphael Pesci – Ecole Nationale Supérieure des Arts et Métiers

**Study of Annular Copper Filled TSVs of Sensor and Interposer Chips for 3D Integration**
Cao Li and Peng Fei – Huazhong University of Science & Technology; Sheng Liu and Huai Zheng – Wuhan University

**On the Process-History Dependence of Package Mechanical Performance**
Ming Wang, Lou Nicholis, MiNa Mo, MinJae Lee, Quan Pham, and Yong Song – Amkor Technology

**Investigations on the Pumping Behaviors of Copper Filler in TSV**
Fei Su and Xiaoxu Pan – Beijing University of Aeronautics and Astronautics

**Warpage Prediction Methodology of Extremely Thin Packages**
Peng Chen, Zhongli Ji, Yangming Liu, Anna Wu, Ning Ye, and Hem Takiar – SanDisk

**Design and Fabrication of Multi-Frequency Antenna using Genetic Algorithms for 5G Applications**
Vincen Gokaj, John Doroshewitz, and Premjeet Chahal – Michigan State University

**Cu-In-Microbumps for Low-Temperature Bonding of Fine-Pitch Interconnects**
Steffen Bickel, Juliana Panchenko, Joerg Meyer, and Volker Neumann – Technical University Dresden;
Wieland Wahrmund and M. Juergen Wolf – Fraunhofer IZM

**A Robust, Stretchable, Capacitive Strain Sensor Fabricated from Silver-Polymer Composite and Urethane Adhesive**
Todd Houghton, Jignesh Vanjaria, Thomas Murphy, and Hongbin Yu – Arizona State University

**Via-in-Trench: A Revolutionary Panel-Based Package RDL Configuration Capable of 200-450 I/O/mm/layer, an Innovation for More-than-Moore System Integration**
Fuhai Liu, Chandrasekharan Nair, Hao Lu, Rui Zhang, Hang Chen, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Atsushi Kubo and Tomoyuki Ando – Tokyo Ohka Kogyo; Kwon Sang Lee – Disco Corporation

**Simulation Analysis of a Conformal Patch Sensor for Skin Tension and Swelling Detection**
Ruiq Lin, Ming-Yuan Cheng, Ramona Damalerio, Wego Guan, and Kwan Ling Tan – Institute of Microelectronics, A*Star

**Effect of Material Properties of Double Layer Non-Conductive Films (D-NCFs) on the Relflow Reliability of Ultra Fine-Pitch Cu-Pillar/Sn-Ag Micro Bump Interconnection**
SeYong Lee, JiWoon Shin, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology; Woojeong Kim and Taejin Choi – Doosan Corporation
Interactive Presentations: Thursday, June 1, 2:00 p.m. - 4:00 p.m and Friday, June 2, 8:30 a.m. - 10:30 a.m.

Wafer-Level Micro Alkali Vapor Cells with Anti-Relaxation Coating Compatible with MEMS Packaging for Chip-Scale Atomic Magnetometers
Yu Ji and Jintang Shang – Southeast University

Low-Temperature High-Throughput Assembly Technology for Transducer Array in Medical Imaging Applications
Hoang-Vu Nguyen, Nu Bich Duyen Do, and Knut Aasmundtveit – University College of Southeast Norway

Highly Efficient and Stable Quantum Dot Light Emitting Diodes Optimized by Micro-Packaged Luminescent Microspheres
Kai Wang and Xiaowei Sun – Southern University of Science and Technology; Xiaobing Luo – Huazhong University of Science and Technology; Sheng Liu – Wuhan University

An Experimental Magnesium Ion Battery Cell Made of Flexible Materials
Todd Houghton, Gamal Eltohamy, and Hongbin Yu – Arizona State University

Friday, June 2, 2017
Session 41: Student Interactive Presentations
8:30 a.m. - 10:30 a.m.
Committee: Interactive Presentations
Session Co-Chairs:
Yu-Lung Huang and Wei-Chih Lin – National Sun Yat-Sen University

Stress Analysis of Flexible Packaging for the Integration of Electronic Components within Woven Textiles
Menglong Li, John Tudor, Russel Torah, and Steve Beeby – University of Southampton

Signal Integrity Analysis of Silicon/Glass/Organic Interposers for 2.5D/3D Interconnects
Sumin Choi and Joungho Kim – Korea Advanced Institute of Science and Technology; Heeong Kim – Missouri S&T; Kyeyong Kim – Samsung Electronics Company, Ltd.

A Study on the Fabrication of Electrical Circuits on Fabrics using Cu Pattern Laminated B-stage Adhesive Films for Electronic Textile Applications
Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

Electrically Testing Non-underfilled Flip Chip Assemblies - Impacts on Interconnect Integrity
Antoine Cloutier and David Danovitch – Université de Sherbrooke; Benoit Foisy – IBM Corporation

Effects of Anisotropic Conductive Films (ACFs) Gap Heights on the Bending Reliability of Chip-in-Flex (CIF) Packages for Wearable Electronics Applications
Ji-Hye Kim, Tae-Ik Lee, Dal-Jin Yoon, Taek-Soo Kim, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

A Study on the Fine Pitch Flex-on-Flex (FOF) Assembly using Flux Added Nanofiber Solder Anisotropic Conductive Films (ACFs) and Thermo-compression Bonding Method
Ji-Soo Lee, Ji-Hye Kim, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

Infrared (IR) Soldering of Metallic Nanowires
Jiří Wang, Fan Gao, and Zhiyong Gu – University of Massachusetts Lowell

Highly Stretchable Electrical Conductive Composites Fabricated from Conducting Polymer Networks and Silver Nanostructures for Wearable Electronics
Bo Song, Kyoung-sik Moon, and C. P. Wong – Georgia Institute of Technology

Numerical and Experimental Study of Fan-out Wafer Level Package Strength
Cheng Xu and Zhaowei Zhong – Nanyang Technological University; Won Kyoung Choi – STATS ChipPAC, Inc.

Effects of Passivation Layer and Electroplating Parameters of Copper Film on Wafer Warpage During Thermal Process
Gong Cheng, Heng Li, Weibo Zhang, Gaowei Xu, and Le Luo – Shanghai Institute of Microsystem and Information Technology

Development of Mechanical Locking Micro-Anchor Structures for qQFN Package Application
Yu-Lung Huang and Wei-Chih Lin – National Sun Yat-Sen University

Investigation of Shear Strength and Fracture Behavior for Cu-Sn Full IMCs Solder Joints with Different Proportion of Cu3Sn
Peng Yao, Xiaoyan Li, Xiaobao Liang, Yang Li, and Fengyang Jin – Beijing University of Technology

Reliability of Cu/NiFe and Cu/Ni Metaconductor Devices for RF Applications
Timothy Clingenpeel and Yong-Kyu Yoon – University of Florida

A New Fan-Out Package Structure Utilizing the Self-Alignment Effect of Molten Solder to Improve the Die Shift and Enhance the Thermal Properties
Hwan-Pil Park, Jae-Yong Park, Gwancheol Seo, and Young-Ho Kim – Hanyang University

Toughening Underfills by Stress-Absorbing Core-Shell Fillers
Chia-Chi Tuan, Kyoung-Sik Moon, and Ching-Ping Wong – Georgia Institute of Technology

Thermal Characteristic of Sn-MWCNT Nanocomposite Solder in LED Package
Choong-Jae Lee, Jae-Jung Moon, Kwang-Ho Jung, and Seung-Boo Jung – Sungkyunkwan University

An Evaluation of Effects of Molding Compound Properties on Reliability of Ag Wire Components
Keisuke Yawaza – Purdue University; Carol Handwerker, John Blendell, Alexander Campbell, Wenhao Chen, Azzedin Jackson, and Matthias Parsons – Purdue University; Peng Su – Juniper Networks

A Nonlinear Transmission Line-Based Harmonic RF Tag for Buried Plastic Pipes
Mohan Iyvat Mohd Ghazali, Saranraj Karuppuswami, Amanpreet kaur, and Premjeet Chahal – Michigan State University

Numerical Analysis and Optimization of Thermal Performance of LED Filament Light Bulb through Phosphors Geometry
Jie Lu, Huai Zheng, and Sheng Liu – Wuhan University; Chunchun Cai, Mengzhong Bao, and Hongbo Wang – Huazhong University of Science and Technology

Effective and Efficient Modeling of Differential Vias Using Semi-Empirical Approach
Fanghui Ren – Oregon State University; Kevin Cai, Chunshun Cui, Jayaprakash Balachandran, and Bidyut Sen – Cisco Systems, Inc.

Design of Low-Profile Integrated Transformer and Inductor for Substrate-Embedding in 1-5kW Isolated GaN DC-DC Converters
Hakaun Lee, Vanessa Smet, Pulugurtha Markondeya Raj, and Rao Tummala – Georgia Institute of Technology

A Stretchable Capacitive Strain Sensor Based on a Novel Polymer Composite Blend
Todd Houghton, Jignesh Vanjara, Thomas Murphy, and Hongbin Yu – Arizona State University

3D Glass Package for Miniaturized Automotive Image Sensing System for Collision Avoidance
Daniel Struk, Peter Hesketh, Chintant Buch, Klaus Wolter, and Rao Tummala – Georgia Institute of Technology

Temperature Stabilization of Pulsed Devices using IMT Thin Films
Michael Fish, Yangang Liang, Xiaohang Zhang, Patrick McCluskey, and Ichiro Takeuchi – Georgia Institute of Technology

Miniaturization of Planar Packaged Inductor using NiZn and Low-Cost Screen Printing Technique
Colin Pardue, Mohamed Bellaredj, Anto Davis, and Madhavan Swaminathan – Georgia Institute of Technology
Today’s hi-tech companies are being very selective in choosing the conferences and trade shows where they will exhibit their products and services. Each year more companies have determined that ECTC provides the opportunity to identify superior prospects. The primary reason is that the engineers and managers who attend ECTC hold decision-making positions at the world’s leading electronics equipment and component manufacturers. The attendees are attracted by ECTC’s strong technical program. Authors in the field believe that ECTC offers the best forum for presenting their work. Exhibit hours will be from 9:00 AM to Noon and 1:30 to 6:30 PM on Wednesday, May 31, and 9:00 AM to Noon and 1:30 to 4:00 PM on Thursday, June 1. All booths in the exhibit hall have been reserved, with this year having a record number of Exhibitors.

Following is a list of exhibitors as of Feb. 1, 2017. The Exhibit Brochure, a current exhibitor list, and a booth layout showing the available booths can be found on the ECTC web site at www.ectc.net under the heading Exhibits. If you need additional information or have questions, call Joe Gisler at +1-480-288-6660, or email gislerhj@mediacombb.net.

2017 TECHNOLOGY CORNER EXHIBITS

HOW TO REGISTER FOR ECTC

By Internet:
Submit your registration electronically via www.ectc.net. Your registration must be received by the cutoff date, May 4, 2017, to qualify for the early registration discounts.

You may contact our registration staff at lrenzi@renziandco.com for additional information. Payment can be made by Visa, MasterCard, or American Express.

Hotel Reservations

1) Contact The Walt Disney World Swan and Dolphin Resort at +1- 888-828-8850. (Reference the ECTC Conference to receive the conference rate of $189/night. In addition, please request your room be reserved in the Walt Disney World Dolphin Resort as the Swan and Dolphin are two separate buildings.)

2) Log onto www.ectc.net and click on the Location tab near the top of the page to find a special online hotel registration link.

The reservation cutoff is Friday, May 5, 2017. All reservations made after the cutoff date of Friday, May 5, 2017, at 5pm ET will be accepted on a space and rate available basis.

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for the 2017 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2017 from 3rd party companies. These emails and sites are not to be trusted. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee.

ECTC’s only authorized site for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that have personally used in the past to book travel. Please be advised, there are scam artists out there, and if it’s too good to be true, it likely is. Should you have any questions about booking a hotel room, please contact ECTC staff at lrenzi@renziandco.com.
### 2017 ECTC Conference Registration Information

<table>
<thead>
<tr>
<th>Conference Registration</th>
<th>Advance Registration</th>
<th>Door Registration</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEEE Member</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attendee (full ECTC conference)</td>
<td>US$730</td>
<td>US$835</td>
</tr>
<tr>
<td>Attendee (Joint ECTC + Itherm conferences)</td>
<td>$945</td>
<td>$1100</td>
</tr>
<tr>
<td>Attendee One-Day Registration</td>
<td>$550</td>
<td>$550</td>
</tr>
<tr>
<td>Speaker or Chair (full ECTC conference)</td>
<td>$605</td>
<td>$730</td>
</tr>
<tr>
<td>Speaker or Chair One-Day Registration</td>
<td>$415</td>
<td>$415</td>
</tr>
<tr>
<td>Non-IEEE Member</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attendee (full ECTC conference)</td>
<td>$920</td>
<td>$1025</td>
</tr>
<tr>
<td>Attendee (Joint ECTC + Itherm conferences)</td>
<td>$1050</td>
<td>$1310</td>
</tr>
<tr>
<td>Attendee One-Day Registration</td>
<td>$550</td>
<td>$550</td>
</tr>
<tr>
<td>Speaker or Chair (full ECTC conference)</td>
<td>$605</td>
<td>$730</td>
</tr>
<tr>
<td>Speaker or Chair One-Day Registration</td>
<td>$415</td>
<td>$415</td>
</tr>
<tr>
<td>Student</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attendee or Speaker (full conference)</td>
<td>$315</td>
<td>$315</td>
</tr>
</tbody>
</table>

### Exhibits

<table>
<thead>
<tr>
<th></th>
<th>Advance Registration</th>
<th>Door Registration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Access to Exhibits Only (not attending conference)</td>
<td>$25</td>
<td>$25</td>
</tr>
<tr>
<td>Exhibit Booth Attendant</td>
<td>$0</td>
<td>$0</td>
</tr>
</tbody>
</table>

### Professional Development Courses (PDCs)

<table>
<thead>
<tr>
<th></th>
<th>Advance Registration</th>
<th>Door Registration</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEEE Member</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full PDC (both a.m. and p.m.)</td>
<td>$605</td>
<td>$710</td>
</tr>
<tr>
<td>Single PDC (a.m. or p.m.)</td>
<td>$420</td>
<td>$500</td>
</tr>
<tr>
<td>Non-IEEE Member</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full PDC (both a.m. and p.m.)</td>
<td>$655</td>
<td>$710</td>
</tr>
<tr>
<td>Single PDC (a.m. or p.m.)</td>
<td>$440</td>
<td>$500</td>
</tr>
<tr>
<td>Student</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full PDC (both a.m. and p.m.) or Single PDC</td>
<td>$130</td>
<td>$130</td>
</tr>
</tbody>
</table>

### Other Registration Options

<table>
<thead>
<tr>
<th></th>
<th>Advance Registration</th>
<th>Door Registration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Extra Proceedings</td>
<td>$100</td>
<td>$100</td>
</tr>
<tr>
<td>Extra Luncheon Tickets</td>
<td>$65</td>
<td>$65</td>
</tr>
<tr>
<td>Cancellation Fee</td>
<td>$50</td>
<td>$50</td>
</tr>
</tbody>
</table>

**Please log onto www.ectc.net/registration to register for the 2017 ECTC.**

There will be no refunds or cancellations after May 4, 2017. Please note that a $50 cancellation fee will be in effect for all cancellations made on or prior to May 4, 2017. Substitutions can be made at any time.

For additional information about registration or ECTC please contact us at:

Renzi & Company, Inc. • Phone: +1-703-863-2223 • Email: renziandco2@gmail.com

*If you join IEEE BEFORE you register for the 2017 ECTC, you can save on registration fees and get free add-on membership to the Components, Packaging and Manufacturing Technology (CPMT) Society for one year!

To take advantage of this offer, simply go to: http://www.ieee.org/go/CPMT_professional

At destination, create your IEEE web account. Once complete, proceed to the Shopping Cart and enter **CPMT2017FREE** in the promotion code box. Click “Apply” and the Shopping Cart will be updated to show the discount. Use your new IEEE membership ID number to register for ECTC at the discounted IEEE Member Rate.

*Non-IEEE members can join IEEE and save $100 or more on ECTC registration and receive CPMT Society membership free for 2017. IEEE members can join the CPMT Society free for the remainder of 2017 with ECTC registration.*
### CONFERENCE SPONSORS

#### Gold Gala Sponsors

- **www.amkor.com**
- **www.cadence.com**
- **www.decatechnologies.com**
- **www.dowelectronicmaterials.com**
- **www.lintec-usa.com/**
- **www.nanium.com**
- **www.pactech.com**
- **www.spts.com**
- **www.unity-sc.com/en/**

#### Silver Gala Sponsors

- **www.appliedmaterials.com**
- **www.ibm.com**
- **www.micron.com**
- **www.spil.com.tw**
- **www.suss.com**
- **www.veeco.com/technologiesandproducts/precisionsurfaceprocessingystems**

#### Special & Program Sponsors

- **www.aseglobal.com**
- **www.brewersscience.com**
- **www.lamresearch.com**
- **www.yieldengineering.com**
<table>
<thead>
<tr>
<th>Wednesday Luncheon Sponsor</th>
<th>Friday Luncheon Sponsor</th>
<th>Badge Lanyard Sponsor</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASE GROUP</td>
<td>JICET</td>
<td>HD MicroSystems</td>
</tr>
<tr>
<td>Tote Bags Sponsor</td>
<td>Intel Student Paper Sponsor</td>
<td></td>
</tr>
<tr>
<td>EMD PERFORMANCE MATERIALS</td>
<td>Intel</td>
<td></td>
</tr>
<tr>
<td>Internet Sponsor</td>
<td>Thumb Drive Sponsor</td>
<td></td>
</tr>
<tr>
<td>Camtek</td>
<td>SPIL</td>
<td></td>
</tr>
<tr>
<td>Refreshment Break Sponsors</td>
<td>Media Sponsors</td>
<td></td>
</tr>
<tr>
<td>AGC</td>
<td>Official Media Sponsor</td>
<td></td>
</tr>
<tr>
<td><a href="http://www.agcem.com">www.agcem.com</a></td>
<td>Chip Scale Review</td>
<td></td>
</tr>
<tr>
<td>ATOTECH</td>
<td><a href="http://www.atotech.com">www.atotech.com</a></td>
<td><a href="http://www.chipscalereview.com">www.chipscalereview.com</a></td>
</tr>
<tr>
<td><a href="http://www.atotech.com">www.atotech.com</a></td>
<td>Additional Media Sponsors</td>
<td></td>
</tr>
<tr>
<td>FUJIFILM</td>
<td>i-Micronews</td>
<td><a href="http://www.i-micronews.com">www.i-micronews.com</a></td>
</tr>
<tr>
<td><a href="http://www.fujifilmusa.com">www.fujifilmusa.com</a></td>
<td>3DInCites</td>
<td><a href="http://www.3dincites.infoneedle.com">www.3dincites.infoneedle.com</a></td>
</tr>
<tr>
<td>INEMI</td>
<td>Circuits Assembly</td>
<td><a href="http://www.circuitassembly.com">www.circuitassembly.com</a></td>
</tr>
<tr>
<td><a href="http://www.inemi.org">www.inemi.org</a></td>
<td>Electronics Cooling</td>
<td><a href="http://www.electronics-cooling.com">www.electronics-cooling.com</a></td>
</tr>
<tr>
<td>Namics</td>
<td>Magnetics</td>
<td><a href="http://www.magneticsmagazine.com">www.magneticsmagazine.com</a></td>
</tr>
<tr>
<td><a href="http://www.namics.co.jp/e/">www.namics.co.jp/e/</a></td>
<td>MEMS Journal</td>
<td><a href="http://www.memsjournal.com">www.memsjournal.com</a></td>
</tr>
<tr>
<td>Qualcomm</td>
<td>SEMICONDUCTOR PACKAGING NEWS</td>
<td></td>
</tr>
<tr>
<td><a href="http://www.qualcomm.com">www.qualcomm.com</a></td>
<td>SoliD State Technology</td>
<td><a href="http://www.electroiq.com">www.electroiq.com</a></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Media sponsors</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
CONFERENCE OVERVIEW

May 30, 2017
Morning Professional Development Courses
8:00 a.m. - 12:00 Noon
1. Achieving High Reliability of Lead-Free Solder Joints – Materials Considerations
2. Wafer Level-Chip Scale Packaging
3. LED Packaging, System, and Reliability Considerations
4. Future of Device and Systems Packaging: Strategic Technologies, Manufacturing Infrastructure, and Applications
5. Polymers and Nanocomposites for Electronic and Photonic Packaging
6. Integrated Thermal Packaging and Reliability of Power Electronics
7. Fundamentals of Electrical Design and Fabrication Processes of Interposers, including their RDLs
8. Introduction to Mechanics Based Quality and Reliability Assessment Methodology

Afternoon Professional Development Courses
1:15 p.m. - 5:15 p.m.
10. Flip Chip Technologies
11. Package Failure Analysis - Failure Mechanisms and Analytical Tools
12. 3D IC Integration and 3D IC Packaging
13. Flexible Hybrid Technologies
14. Polymers for Electronic Packaging
15. Emerging Interconnect and System Integration Technologies
16. Package Failure Mechanisms, Reliability, and Solutions
17. Ageing of Polymers and the Influence on Microelectronic Package Reliability
18. Thermo-Electrical Co-Design for 3D Integration

Technical Subcommittee Special Session
10:00 a.m. - 11:30 a.m.
“Material and Package Reliability Needs/Challenges for Harsh Environments”

ECTC Special Session
2:00 p.m. - 3:30 p.m.
“Flexible Hybrid Electronics – Electronics Outside the Box”

ECTC Panel Session
7:30 p.m. - 9:00 p.m.

May 31, 2017
Technical Sessions
8:00 a.m. - 11:40 a.m.
1. Fan-Out Packaging Process and Integration
2. TSV Process, Characterization and Applications
3. Flip Chip Assembly
4. Advanced Substrates and Integrated Devices
5. Emerging Sensors and Microsystems Packaging
6. 5G, mmWave and Beyond

Interactive Presentation Sessions 37 & 38
9:00 a.m. - 11:00 a.m.
2:00 p.m. - 4:00 p.m.

Technical Sessions
1:30 p.m. - 5:10 p.m.
7. Fan-Out Packaging Materials and Passives
8. Singulation Process Developments
10. Harsh Environment Interconnect Reliability
11. Mechanical Modeling and Characterization of Interposers and Interconnections
12. Advanced Optical Components and Modules

CPMT Women's Panel and Reception
6:30 p.m. - 7:30 p.m.
“Emotional Intelligence (EI) - Link to Successful Leadership”

ECTC Plenary Session
7:30 p.m. - 9:00 p.m.
“Packaging for Autonomous Vehicle Electronics”

June 1, 2017
Technical Sessions
8:00 a.m. - 11:40 a.m.
13. Interconnect Advances in FO & WLP
14. Heterogeneous Integration
15. Flip Chip and Embedding in Substrates
16. 3D Materials and Processing
17. Materials and Processes for Flexible and Wearable Devices
18. Warpage, Electromigration and Mechanical Characterization

Interactive Presentation Sessions 39 & 40
9:00 a.m. - 11:00 a.m.
2:00 p.m. - 4:00 p.m.

Technical Sessions
1:30 p.m. - 5:10 p.m.
19. Recent Advances in FOWLP Technology
20. MEMS and Sensor Technologies
21. 3D Cu-Cu and Micro Bump Bonding Technologies
22. Solder Joint & Interconnect Reliability, Characterization and Modeling
23. Additive Manufacturing and Panel-Level Packaging
24. Novel Methods to Assess Reliability

Session Summary by Interest Area

3D/TSV Topics
S2, S16, S21, S26, S32

Advanced Packaging
S1, S7, S14, S15, S20, S26, S31

Applied Reliability
S10, S24, S25, S32

Assembly & Manufacturing Technology
S3, S8, S14, S29

Emerging Technologies
S5, S17, S23

High-Speed, Wireless & Components
S6, S30, S36

Interconnections
S2, S9, S13, S21, S27, S32

Materials & Processing
S4, S16, S19, S28, S33

Thermal/Mechanical Simulation & Characterization
S11, S18, S22, S35

Optoelectronics
S12, S34

Interactive Presentations
S37, S38, S39, S40, S41

CPMT Seminar
8:00 p.m. - 9:30 p.m.
“3D Printing Tools, Technologies and Applications”

June 2, 2017
Technical Sessions
8:00 a.m. - 11:40 a.m.
25. Characterization and Reliability of Fan-Out & WLP
26. 3D Integration Processing and Reliability
27. Advances in Thermal Compression and Wirebonding
28. Advanced Materials for Reliability Improvement
29. Warpage Control and Substrates
30. RF Components and Module Integration

Student Interactive Presentations Session 41
8:30 a.m. - 10:30 a.m.

Technical Sessions
1:30 p.m. - 5:10 p.m.
31. Auto Electronics Packaging and Power Modules
32. Reliability Challenges in 2.5D/3D Interconnect
33. Advanced Bonding and Soldering Technology
34. Waveguide Devices and Chip-to-Fiber Packaging
35. Thermomechanical and Thermal Characterization
36. Advances in Signal and Power Integrity
Mark Your Calendar for ECTC 2018

Sheraton San Diego Hotel & Marina
San Diego, California, USA
May 29 - June 1, 2018