STMicroelectronics Technology offer through CMP in 2020
Deep Sub-Micron, SOI and SiGe Processes
https://mycmp.fr
CMP Process Portfolio from ST

- **Low Power & High Speed Digital, RF**
  - 28nm FDSOI: 28FDSOI

- **Optical, Wireless, Analog High Performance**
  - 55nm SiGe: BiCMOS055

- **Advanced Mixed A/D, RF**
  - 65nm CMOS: CMOS065LPGP

- **High Voltage Applications**
  - 160nm CMOS: SOIBCD8s
  - 160nm CMOS: BCD8SP

- **Mixed A/D, RF**
  - 130nm SiGe: BICMOS9MW
  - 130nm SOI: H9SOI-FEM
  - 130nm HV-CMOS: HCMOS9A
  - *Energy Harvesting (H9A-EH)*
28nm: FDSOI28

28nm FDSOI: Fully depleted Silicon On Insulator:

- 28nm mixed A/D/RF CMOS SLP/8LM (triple Well).
- Gate length: 28nm.
- 8 Cu metal layers (6 thin + 2 thick Cu top metal).

Body Biasing
- Performance – Leakage balance
- Process compensation

- IO supply voltage: 1.8 V using the IO oxide.
- Ultra low k inter-level dielectric.
- Low leakage (High density) SRAMS.
- Analog / RF capabilities.
- MIM and Fringe MOM capacitors.
- Standard cell libraires (more than 3Mgates/mm²).

2 MPW runs forecast in 2020: 10th February, 14th September.
Starting price: 9000€/mm² for 40 samples and 6750€/mm² for circuit above 2mm².
Turnaround: 24 weeks to 32 weeks.
Current supported version of the design kits: 1.2

Applications: Low power and high performance applications
SiGe 55nm: BiCMOS055

- **55nm BiCMOS055 SiGe: Low Power:**
  - 55nm mixed A/D/RF CMOS SLP/8LM (triple Well)
  - Gate length: 55nm (drawn)
  - 8 Cu metal layers
  - Ultra-thick Cu top metal
  - Bipolar SiGe-C NPN transistors with $F_t = 320$ GHz
  - Low Power and General purpose MOS transistor
  - Dual gate oxide (1V for core, 2.5V and 3.3V for IO)
  - MIM and Fringe MOM capacitors
  - TFR (Thin Film Resistor)
  - High density of integration: up to 970k gates/mm²
  - Various power supplies: 2.5V, 1.2V, 1V
  - Millimeter-wave inductor

2 MPW runs forecast in 2020: **17th February, 27th July.**

Starting Price: **5500€/mm² for 40 samples and 4250€/mm² for circuit above 2mm².**

Turnaround: 28 weeks to 36 weeks.

Current supported version of the design kits: **2.8.a**

**Applications:** Optical, Wireless and High-Performance Analog Applications.
Deep Sub-micron 65nm: CMOS65LPGP

- **65nm CMOS65LPGP CMOS: Low Power General Purpose:**
  - 65nm mixed A/D/RF CMOS SLP/7LM (triple Well).
  - Gate length: 65nm.
  - 7 Cu metal layers.
  - High Density of integration: 800kgates/mm².
  - RF kit available on request and subject to restriction.
  - Dual gate oxide (1V for core and 2.5V for IO).
  - Various Power supplies for Core: 1.2V, 1.0V
  - Various Power supplies for IOs: 3.3V, 2.5V, 1.8V, 1.2V
  - MIM and Fringe MOM capacitors.
  - Multiple $V_t$ transistor offering.
  - Standard cells librairies.

**Applications:** General purpose, Analog/RF capabilities.

2 MPW runs forecast in 2020: **4th February, 5th June**

Starting Price: **4500€/mm² for 40 samples and 3750€ for circuit above 5mm²**.

Turnaround: 22 weeks to 26 weeks.

Current supported version of the design kits: **5.8**
**Sub-micron 130nm: B9MW**

- **130nm BiCMOS9MW SiGe:**
  - 130nm mixed A/D/RF CMOS SLP/6LM (triple Well).
  - BICMOS9MW technology is using 130nm HCMOS9GP as base process.
  - Power supply: 1.2V for core and 2.5V & 3.3V for IO.
  - Threshold voltages: \( V_{TN} = 500/380 \text{ mV}, \ V_{TP} = 480/390 \text{ mV} \)

- 6 Cu Metal layers, thick top metal layer.

- **SiGe-C bipolar transistor** (\( f_T = 230 \text{GHz} \))
  - High performance and Medium voltage NPN bipolar transistor.

- MIM capacitors.
- Damascene Copper from metal 1 to last metal.

- Standard cells libraries

- 3 MPW runs forecast in 2020: 2\textsuperscript{nd} March, 2\textsuperscript{nd} June and 2\textsuperscript{nd} November
- Starting Price: 2600€/mm\(^2\) for 40 samples and 2200€/mm\(^2\) for circuit above 5mm\(^2\)
- Turnaround: 16 weeks to 18 weeks.
- Current supporter version of the Design kits: 2.9b in BiCMOS9MW.

**Applications:** General purpose Analog/Digital/ RF applications and Millimeter-Wave applications (frequencies up to 77GHz for automotive radars), WLAN, Optical communication.
Sub-micron 130nm: H9-SOI-FEM

130nm H9-SOI-FEM: Front-End Module:

- 130nm mixed A/D/RF CMOS SLP/M4TC (Thick Copper Metal Stack).
- Gate length: 130nm.
- Ultra-thick Cu top metal, 4 Cu metal layers.
- 200mm SOI wafers with high resistive (HR) substrate and Trap Rich SOI.

- High Linearity MIM capacitor (2fF/mm²).
- 5.0V NLDMOS & PLDMOS.
- Standard cell libraries & 1.8V IO cells
- Floating body CMOS 5.0V NLDMOS.
- Power supply: 1.2 V

- Body contacted CMOS.
- Address a cost-driven application
- Capability to address all FEM applications (Switches, LNA, PA)

Enabling 802.11 ac LNA integration
- High linearity requirement
- Low NF at 5 GHz

Starting Price: Contact CMP for dedicated run price.
- Turnaround: 16 weeks to 18 weeks.
- Current supported version of the design kits: 14.1

Applications: Radio receiver/transceiver, Cellular, Wifi, Automotive keyless systems.
130nm: HCMOS9A + CEA-LETI NVM

- **130nm HCMOS9A HV-CMOS: Add-on Non Volatile Memory with CEA-LETI**
  - Based on HCMOS9A 130nm mixed A/D/RF technology of STMicroelectronics, and with cooperation of CEA-LETI.
  - CMP opened a new service for Non Volatile Memory integration in 2018.
  - Standard cell Libraries: Core cells, digital IO (1.2V, 1.8V) & 20V Analog IOs and NVM add-on.
  - LETI NVM design kit available from February/March 2018.

**Library name:** Addon_NVM_Lib
- **Category Device:** OxRam

**Applications:** For all applications requiring non-volatile memory.

**1 MPW run forecast in 2020:** 21\(^{st}\) September 2020
**Starting Price:** 4000€/mm\(^2\) for 40 samples and 3200€/mm\(^2\) for circuit above 5mm\(^2\).
**Turnaround:** 24 weeks to 30 weeks (dataprep/Front end ST and post-process CEA-LETI).
**Current supported version of the design kits:** 10.9/2018.4.1
BCD 160nm: BCD8sP

- **160nm BCD8SP**: Bipolar-CMOS-DMOS Smart Power:
  - 160nm Mixed Analog / Digital Bipolar-CMOS-DMOS 4LM.
  - Gate length: 180nm (drawn).
  - 4 Cu metal layers, Thick Power M4, M4 Al optional.
  - Operating voltages: 1.8V - 5V : Digital & Analog.
  - Power devices: 10V - 18V - 27V - 42V - 60V.
  - Dual gate oxide process: 1.8V CMOS, 5V CMOS.

- Analog + Digital + Power & HV on one chip.
  - High power transistor.
  - Low power digital and analog device.


**Applications**: Power Management systems, DC-DC converter, Motor drivers, Printer.

**CMP Contact**: Lyubomir KERACHEV

- 1 MPW run forecast in 2020: **12th March, 1st October**
- Starting Price: **2500€/mm²** for 40 samples, and **2200€/mm²** for circuit above 5mm²
- Turnaround: 18 weeks to 24 weeks
- Current supported version of Design Kits: **2.4.**
BCM annual users' meeting – 30 January 2020

160nm SOIBCD8s: Bipolar-CMOS-DMOS Smart Power on SOI:
- 160nm Mixed Analog / Digital Bipolar-CMOS-DMOS 4LM on SOI
- Gate length: 180nm (drawn).
- 4 Cu metal layers, Al-Cu Thick Power M4.

- Operating voltages: 3.3V baseline, 1.8V optional: Digital & Analog.
  - Medium Voltage Module Power MOS: 6V – 40V.
  - High Voltage Module MOS: 70V – 200V.
  - Dielectric Isolation on SOI.

- Analog + Digital + Power & HV on one chip.
  - High Voltage to drive external loads.
  - Analog block to interface « external world » to the digital systems.
  - Digital Core for signal processing.

• 2 MPW runs forecast in 2020: 16th July
• Starting Price: 2500€/mm² for 40 samples and 2200€/mm² for circuit above 5mm²
• Turnaround: 18 weeks to 24 weeks.
• Current supported version of Design Kits: 2.1

Applications: Automotive Sensor Interface ICs, 3D Ultrasound, MEMS & micro-mirror driver.
RAM and ROM blocks available through STMicroelectronics Memory Generators:

- BCD8SP
- HCMOS9GP
- BICMOS9MW
- HCMOS9A
- CMOS65LP
- CMOS65GP
- CMOS28FDSoI
- BiCMOS55

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<tr>
<th>Technology</th>
<th>SPREG</th>
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## New Prices for 2020

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<th>STANDARD €/mm²</th>
<th>DISCOUNT €/project</th>
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<td>ST 28nm CMOS28FDOSI</td>
<td>9000 ²,⁷</td>
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<td>18000 + [(Area-2) x 6750] ⁵</td>
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<td>ST 55nm BiCMOS055</td>
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<td>11000 + [(Area-2) x 4250] ⁵</td>
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<td>ST 65nm CMOS065</td>
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<td>13000 + [(Area-5) x 2200] ⁶</td>
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<td>11000 + [(Area-5) x 1500] ⁶</td>
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<td>ST 130nm HCMOS9GP</td>
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<td>12500 + [(Area-5) x 2200] ⁶</td>
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### STMicroelectronics Wafer Level Bumping

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Thank You!
BACKUP
### Supported CAD Tools by STMicroelectronics Design kits:

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<tr>
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<th>Electrical Simulation</th>
<th>Verification</th>
<th>Parasitic extraction</th>
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<td>Spectre (CDS)</td>
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<td>ICC (SNPS)</td>
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- HCMOS9GP
- BiCMOS9MW
- HCMOS9A
- H9SOI-FEM
- CMOS065
- BiCMOS55
- CMOS028 FDSOI
- BCD8sP

**CMP annual users’ meeting – 30 January 2020**

Horizon 2020 European Union funding for Research & Innovation
The circuits must be sent to CMP via FTP:
- Circuits should be sent, **with corners cut**, **without sealring** and **without tiling**.
- DRCs should have been run on the gds2 file before being sent. DRC must be clean except low densities outside exclusion area.

**DRC free of error**
- Replacement of ST standard cells
- Data checking + DRC
- Help for corrections (Report)

**Sealring generation**
- Addition of the sealring
- Addition of logos
- Addition of foundry cells

**Tiling**
- Verification of tiled circuit
- Report to the user
- Shipment to ST
Submission cycle for CMP users

- Design transfer
  - Data checking (DRC)
  - Help for corrections (Report)
  - Data preparation (Sealring/Tiling)
  - Supports

- Wafers shipment
  - 12 to 28 weeks Depending on technologies

Users

- Research Laboratories
- Education & Universities
- Companies, Startup

Foundry

- Transfer validated designs

- Report for corrections

2 to 3 weeks

Reservation for MPW run one month before the CMP deadline is mandatory:

- The global turnaround includes the data checking, verifications, supports and final data preparation done at CMP

CMP annual users’ meeting – 30 January 2020