Circuits Multi-Projets®

0.35µm, 0.18µm MPW services

http://mycmp.fr

Grenoble - France

ams Available Processes

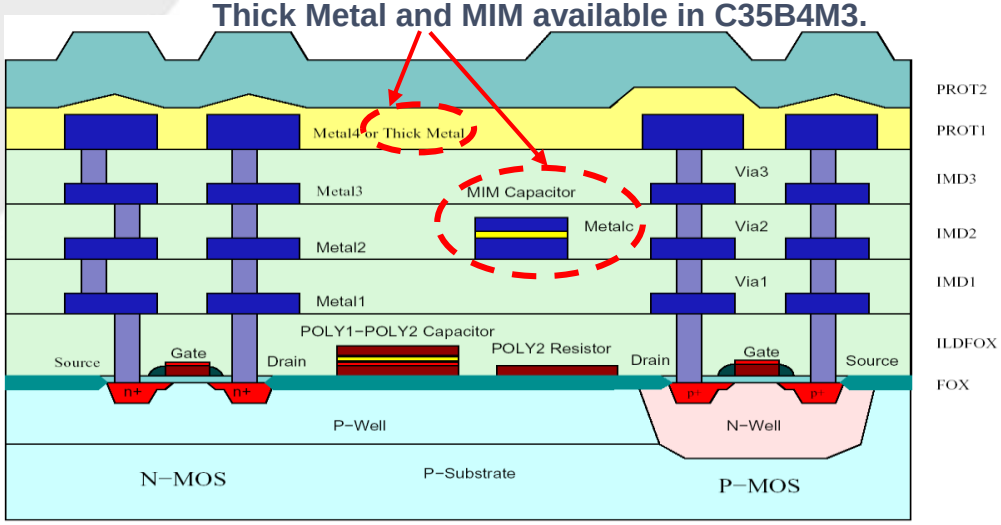
Process Name	Process Feature
C35B4C3	0.35µm CMOS 3.3V / 5.0V
C35B4C2	0.35µm CMOS 3.3V
C35B4O1	0.35µm CMOS-Opto ARC
C35B4OA	0.35µm CMOS-Opto BARC
S35D4M5	0.35µm SiGe BiCMOS
C35B4M3	0.35µm CMOS-RF
H35B4D3	0.35µm HV-CMOS
BYE / BYQ	0.8µm BiCMOS (available on request)

Process (0.35µm CMOS)

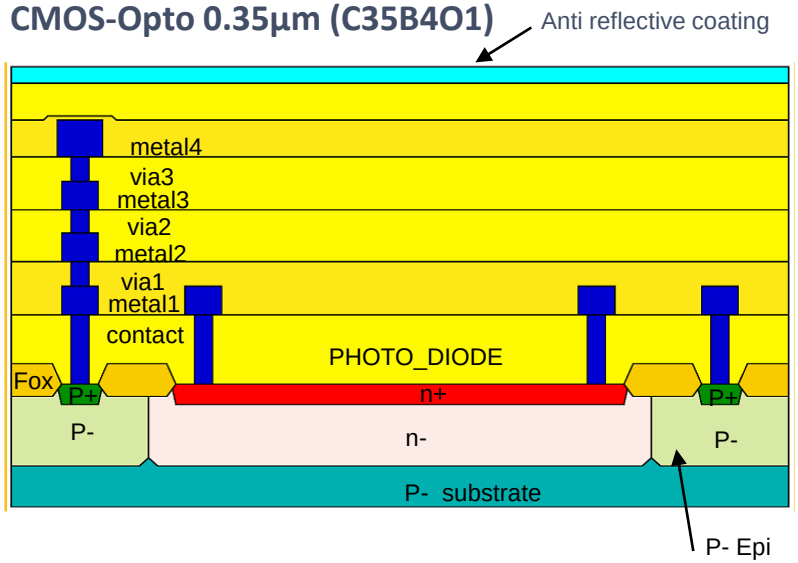
CMOS 0.35µm C35 (C35B4C3)

- 2 Layers Polysilicon, 4 Layers Metal, 3.3V / 5.0V, High Resistive Poly.
- 3.3V / 5.0V I/O pads.
- Peripheral cells with high driving capability (from 1mA to 24mA)
- Application : Analog, Digital, Mixed A/D, RF.
- Density : 18 kgates/mm^2
- Gate Delay: 100ps (NAND2 typical)
- Libraries : Digital and Analog Standard Cells + Pads + P-Cells.
- CORELIB qualified for 1.8V / 2.2V / 2.7V / 3.3V
- CORELIB_V5 qualified for 2.0V / 3.0V / 4.0V / 5.0V

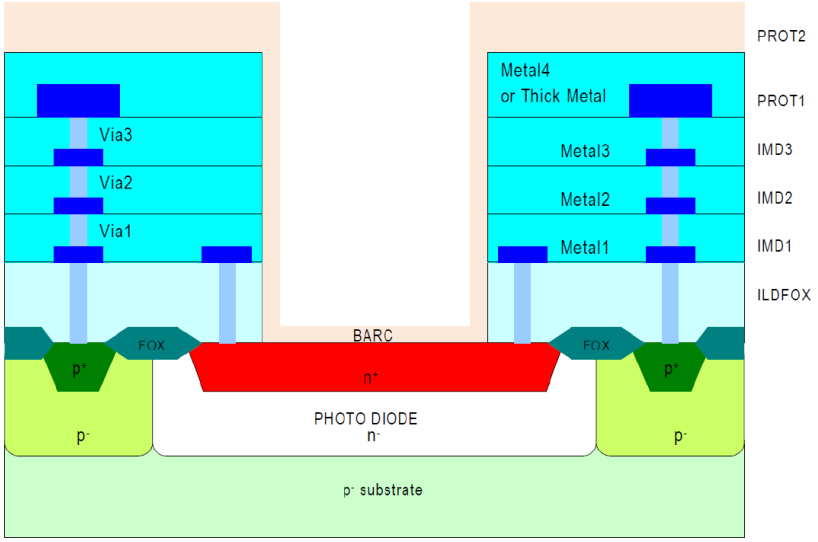
Thick Metal and MIM available in C35B4M3.



CMOS-Opto 0.35µm (C35B4O1)



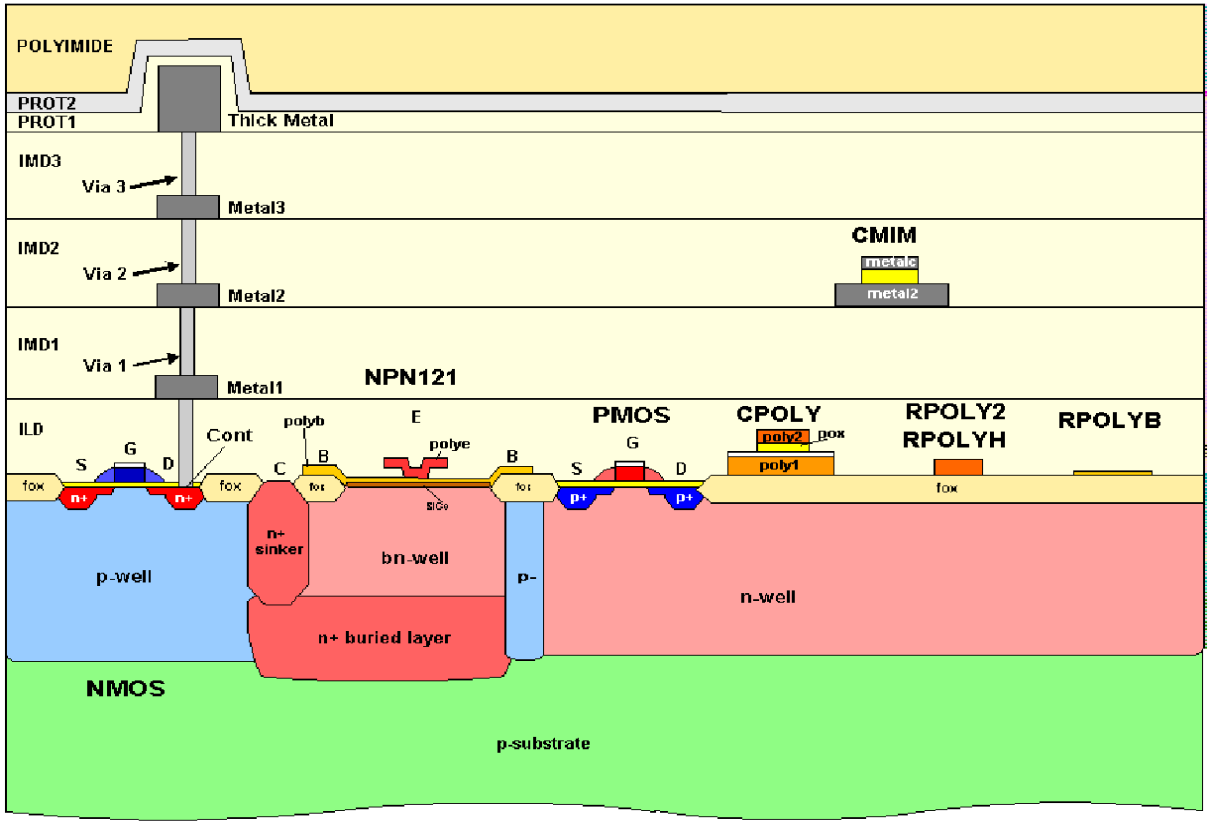
CMOS-Opto 0.35µm (C35B4OA)



amsProcess (0.35µm SiGe)

SiGe HBT-BiCMOS 0.35µm S35D4M5

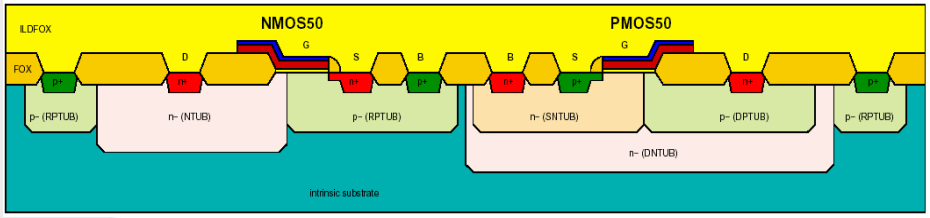
- 4 Layers Polysilicon / 4 Layers Metal.
- Power supply voltage range (2.5V – 3.6V / 5.5V)
- Vertical SiGe-HBT NPN : Ft = 70 GHz
- High Resistive Polysilicon.
- Poly1/Poly2 capacitors
- MIM capacitors
- Thick Top Metal



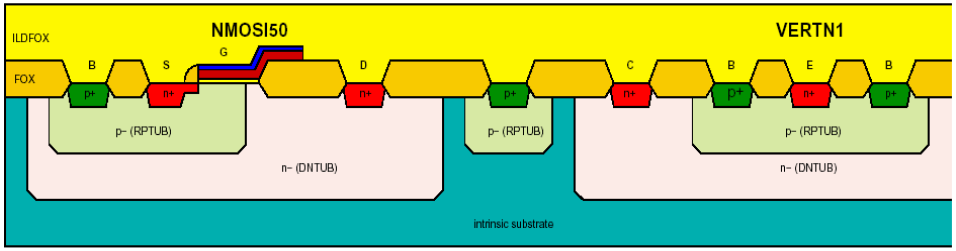
Process (0.35µm HV-CMOS)

HV CMOS 0.35µm **H35 (H35B4D3)**

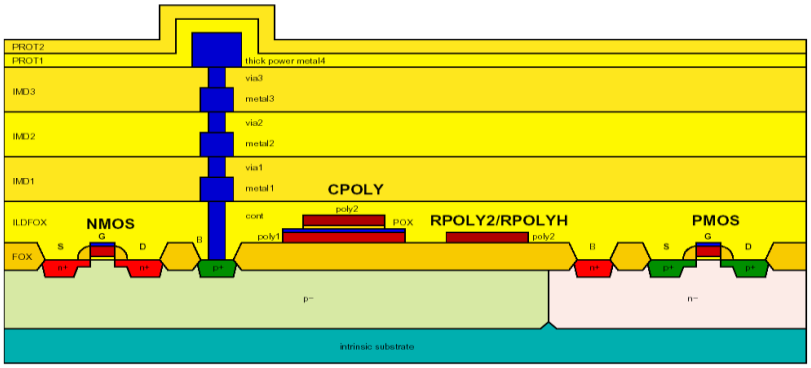
- 2 Layers Polysilicon, 4 Layers Metal, High Resistive Poly, Thick 4th Metal.
- 20V / 50 V / 120 V Maximum operating voltage.
- 3.3V / 5.0V / 20V Maximum gate voltage.
- R_{on} = 0.11 Ohm mm^2 for HV-NMOS
- R_{on} = 0.29 Ohm mm^2 for HV-PMOS



NMOS50 (50V) PMOS50 (50V)
NMOS120 (120V) PMOS120 (120V)

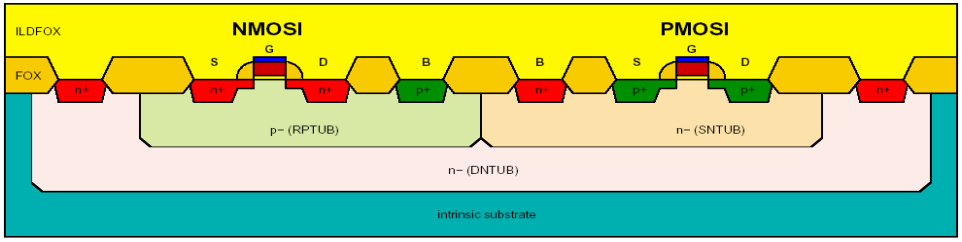


NMOSI50 (50V) VERTN1



Standard 3.3V / 5V

Isolated 3.3V / 5V

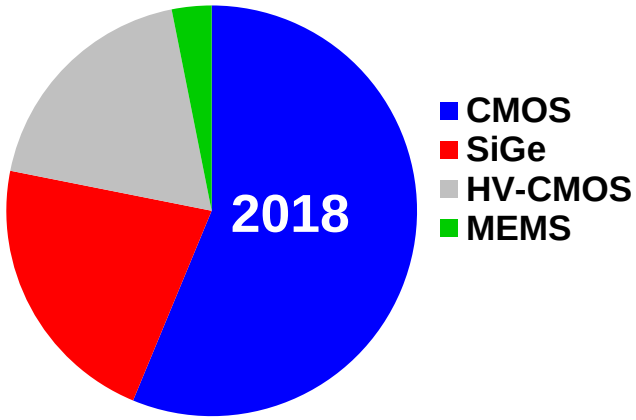


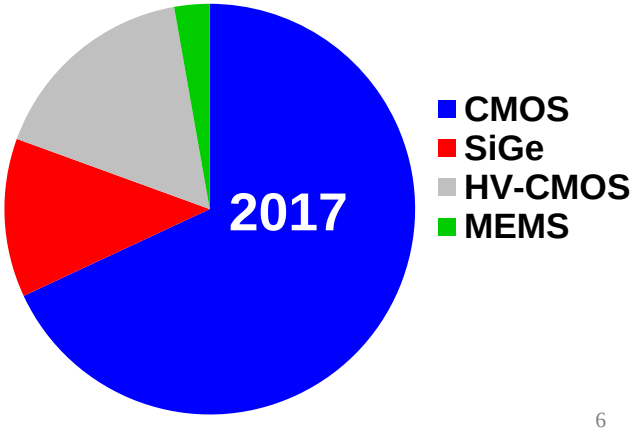
ams Runs in 2018

Number of prototypes in 2018 : 64 (70 in 2017)
Number of Low volume prod. in 2018 : 23 (16 in 2017)

22 scheduled MPW runs (30 in 2017)
14 extra runs (Production) (8 in 2017)

CMOS	36 (47 in 2017)	67% (67% in 2017)
MEMS Bulk-micromachining	2 (2 in 2017)	3% (3% in 2017)
SiGe	14 (9 in 2017)	13% (13% in 2017)
HV-CMOS	12 (12 in 2017)	17% (17% in 2017)





Summary news on the AMS offer at CMP

- New CMP pricing / Discounted price for NEXTS/Europractice members.
- In 2019: 4 MPW runs for CMOS, 2 MPW runs in SiGe, 2 MPW runs in HV.
- Dedicated engineering runs available for new projects, or existing mask-sets.
- 0.8µm BiCMOS is phasing out until December 31st, 2019, then will stop.
- No more 0.18µm CMOS or HV-CMOS offer from AMS since January 2019.

EM 0.18µm Process

EM microelectronic
0.18µm MPW services

COMING SOON

CMP is about to provide access to

em microelectronic

Available Q2 2019

Technology offering overview

	Minimum Gate Length:	Dual Gate Oxides:	# Metal Layers	FEOL Isolation
0.18µm **EMALPC18** logic	180nm [drawn]	3.0nm ThinGOX [1.98V max] 6.5nm DualGOX [3.63V max]	4/5 Metal Layers: AlCu: option B -4 ML or option M -5 ML	Non Epi or p-Epi substrate [16-24Ω.cm] STI [Shallow trench Isolation]

Analog Low Power

- Ultra-Low power
- Low Vth
- Low leakage

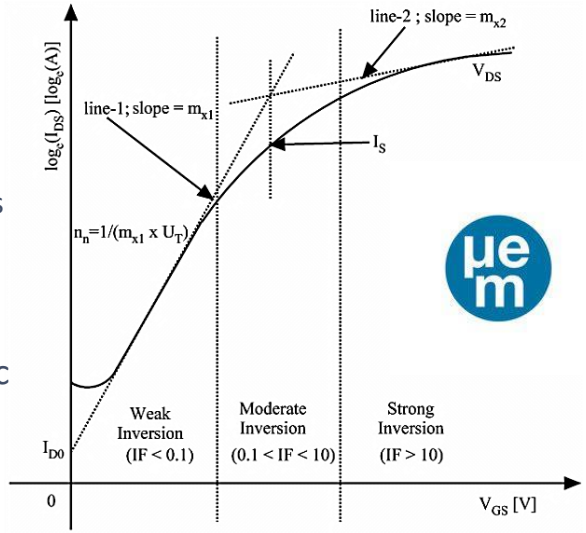
COMING SOON

Price / Schedule / General information

MPW SCHEDULE	A	M	J	J	A	S	O	N	D	Standard price in Euro/mm^2	Discount in Euro/project*
EMALPC18 technology	24			31			30			1950 Euro/mm² for Area < 5mm²	600
										1250 Euro/mm² for mm² above 5mm²	

Price = area (mm²) X price/mm² with minimum fabrication cost equivalent to 2,35 mm²
* For active Europractice IC member only.

- Key features : 8 inch Fab, fully manufactured in Switzerland
  - 180 nm – Including accurate devices, **optimized for Analog**
  - Developed for **Ultra Low Power, Ultra Low Voltage** Designs
  - **EKV accurate** model/parameters for **near threshold** bias
- Ultra low power, horlogy, sensors, IoT, Mixed analog/digital
- Advanced models for accurate simulations, Standard logic & IO cells, advanced devices and IPs
- Dedicated runs available on request



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On Semi 0.18µm & 0.35µm Processes

On Semiconductors
0.18µm & 0.35µm MPW services

COMING SOON

CMP is about to provide access to

ON Semi Custom Foundry

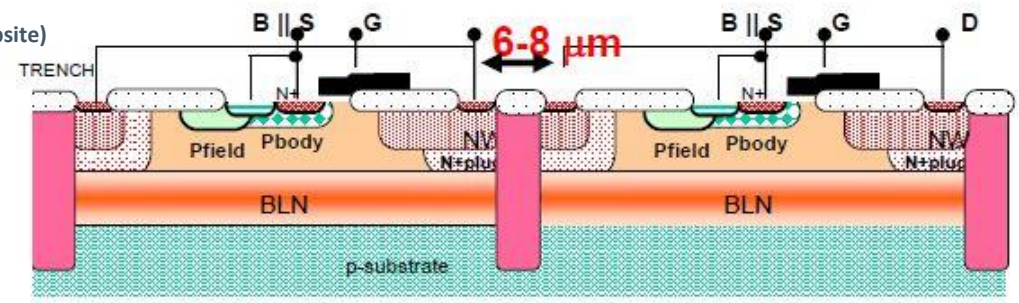
Available Q2 2019

Technology offering overview

ON Semiconductor®	Max Operating Voltage (Vgs)	Max Drain Voltage (Vds)	Tmin/ Tmax	# Metal Layers	Isolation	MEMORIES RAM / ROM / OTP /EEPROM
0.35µm **ONC35U**	3.3 V / 5 V	5 V	-40/+150	3 - 5	Junction	Y [1]
0.35µm **ONC35I3T25U**	3.3 V / 12 V	25 V	-40/+155	3 - 5	Junction	Y [1]
0.35µm **ONC35I3T50U**	3.3 V	50 V	-40/+190	3 - 5	DTI	Y [1]
0.18µm **ONC18MS**	1.8V / 3.3V	15 V	-45/+135 [2]	4 - 6	Junction	Y
0.18µm **ONCI4T**	1.8 V 3.3 V	70 V	-45/+200 [2]	4 - 6	DTI	Y

Notes:
Metal Layer from 3 to 5 available on request.
Intrinsic technology temperature capability : 200°C
Default parameters (Options available on request, listed and described on website)

1 OTP: unsupported but Leaf cells available for I3T50
2 Cryo models for 1.8V and 3.3V MOS (n- and p-type) and resistors



I3T50 cross section

COMING SOON

Price / Schedule / General information

MPW SCHEDULE	A	M	J	J	A	S	O	N	D	Standard price in €/mm²	Discounted price in €/mm²*
0.35µm **ONC35U 4M** including analog options			1			16			2	**720**	**670**
0.35µm **ONC35I3T25U** 3.3/25 V 4M only thick top metal			1			16			2	**770**	**720**
0.35µm **ONC35I3T50U** (E) 50 V 4M (5M on special request)						2			2	**925**	**875**
0.18µm **ONC18MS** (0.18 µm - 1.8/3.3 V - 15V DMOS - 5LM - MiMC - ESD - HiR - EPI)			10		12		7		9	**1100**	**1050**
0.18µm **ONC18I4T** 45/70V HV CMOS (=ONC18MS + 30V + 45V + 70V DMOS)			10		12		7		9	**1540**	**1480**

Price = area (mm²) * price/mm² with minimum fabrication cost equivalent to 10 mm²
*** For active Europractice IC member only.**

ON Semiconductor®

- Industrial and automotive qualified up to Tj 200°C.
- Many options available on requests (check on web-site)
- Extensive ESD library
- MLM (Multi-layer mask set) for POC and qualifications
- SLM (Production mask set)

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