From layout to chips

Flip-Chip & Advanced Packaging Services

Horizon 2020
European Union funding
for Research & Innovation

From layout to chips

Flip-Chip Packaging

- Interconnects on silicon (front side post process)
- Custom substrates
- Flip-Chip assembly

Advanced Packaging

- Silicon Interposer
- OPEN 3D post process for 3D integration

Flip-Chip Packaging

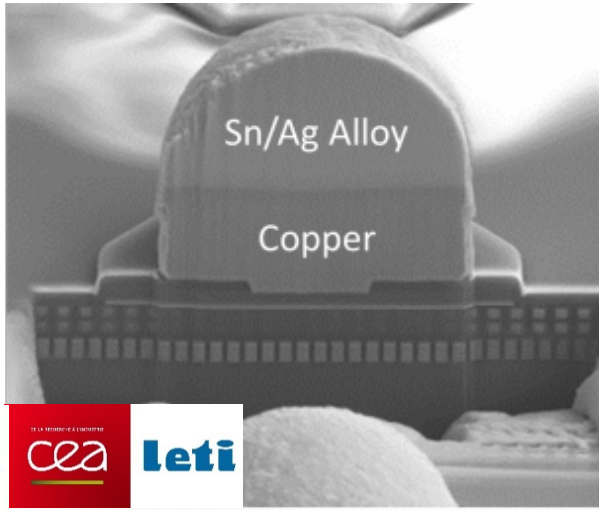
- **Interconnects on silicon (front side post process)**
  - Wafer level: copper pillars and solder bumps
  - Die level: Gold stud bumps and solder bumps
- **Custom substrates**
- **Flip-Chip assembly**

Wafer-level Copper pillars

Copper pillar post-process by CEA-LETI

Features:

- UBM process
- Pillar of copper +Sn/Ag alloy capping
- Low Diameter / Height (25µm / 20µm)
- Very fine pitch (down to 50µm)
- Very suitable for advanced technologies
- Available on any CMP run



Pricing:

- Depending on the silicon process
- Starting at 17k€

Wafer-level Copper pillars

New

Copper pillar post-process by ST microelectronics

Features:

- UBM process
- Pillar of copper + Sn/Ag alloy capping
- **Small** Diameter / Height: 62µm / 65 µm
- **Fine pitch** (down to 90µm)
- Available on **ST 300mm** processes
- **Fast turnaround** (2 weeks)

Courtesy STMicroelectronics

life.augmented

Pricing:

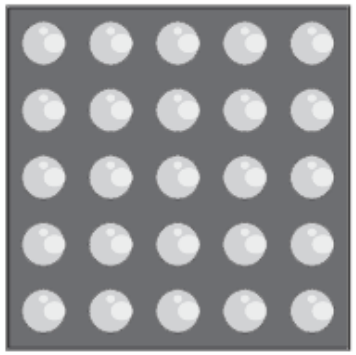
- Depending on the silicon process
- CMOS65: 23k€
- BiCMOS55: 25k€
- 28FDSOI: 33k€

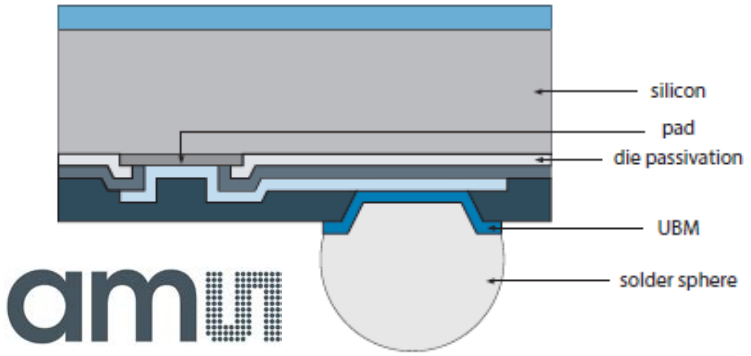
Wafer-level Solder Bumps

Solder bumping service by ams

Features:

- Redistribution Layer (RDL) deposition + UBM
- Solder sphere deposition
- Pitch compatible with **PCB assembly** processes (350µm)
- Available on **any 0.35µm** ams MPW run
- Option is supported **within ams hit kit** upon request





Pricing:

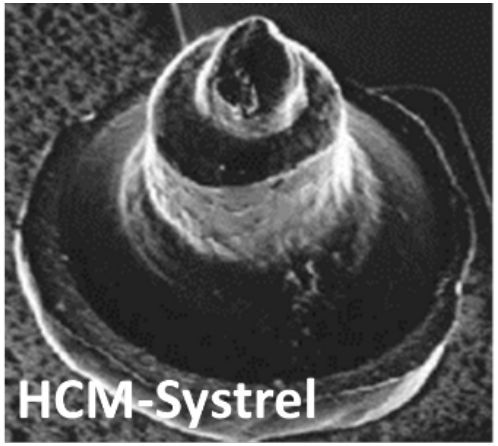
- Flat fee of 6200 € per design (for 40 chips delivered)

Die-level Gold stud bumps

Gold stud bumping services

Features:

- Available on **any project** through CMP
- Realized with **wire-bonding equipment**
- Ball bonded with gold wire
- **No RDL/UBM** required
- **Fast turnaround** (2 weeks)
- Assembly by thermocompression/thermosonic
- Up to ~40 IOs



Pricing:

- Flat fee of **1200 €** for 10 pieces delivered

Die-level Solder Bumps

Solder Bumping services

Features:

- UBM electroless Ni/Au deposition
- Solder ball individual placement (Sn/Ag/Cu alloy)
- Available on any project through CMP
- Increased number of IO
- Assembly by reflow
- Compatible with organic substrates

Pricing:

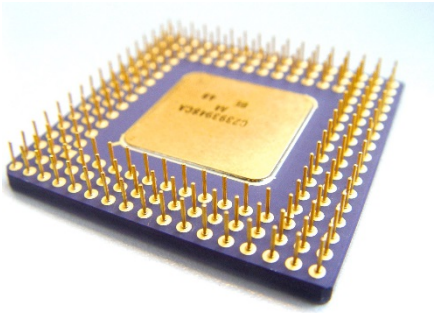
- IO-dependent: 10k€ for 84 IO
- Single die UBM is a manual non-standard process strongly design-dependent that can only be done on best effort delivery from CMP

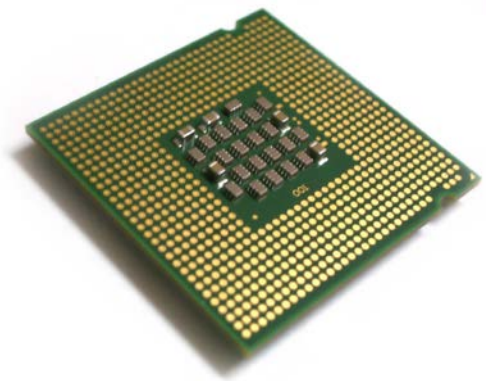
Custom substrates

CMP handles requests for ceramic or plastic custom substrates

Support features:

- Available on **any CMP MPW run**
- **Feasibility study** with subcontractors ensured by CMP
- Die/Substrate **co-design verification** before fabrication
- **Coordination** of the different links of the packaging chain





Pricing:

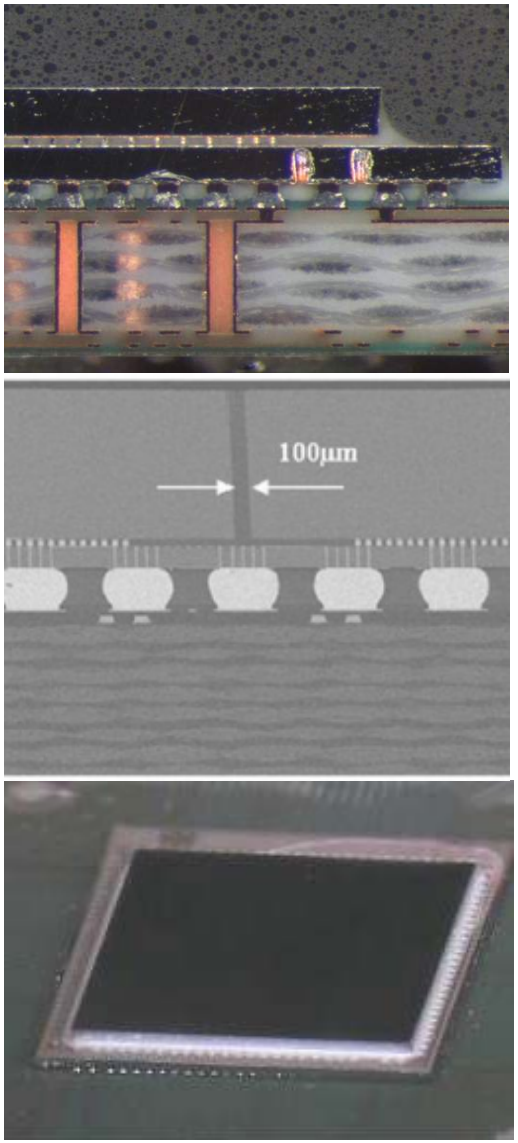
- Depending on substrate specifications

Flip-Chip assembly

Flip-Chip assembly services through CMP:

- Flip-Chip on **custom substrate or directly on PCB**
- **Flip-chip techniques:** thermocompression, thermosonic, reflow
- **Choice** of subcontractors/techniques **depends on:**
  - Chip type
  - Interconnects type
  - Substrate type
- **Available options:** Underfill, Encapsulation, SMD assembly, substrate backside balling…

Anticipation is a key issue during design!
Contact us in the early stages of your project



Source: CEA-Leti/ STMicroelectronics

From layout to chips

Flip-Chip Packaging

- Interconnects on silicon
- Flip-Chip assembly
- Custom substrate

Advanced Packaging

- **Silicon Interposer**
- **OPEN 3D post process for 3D integration**

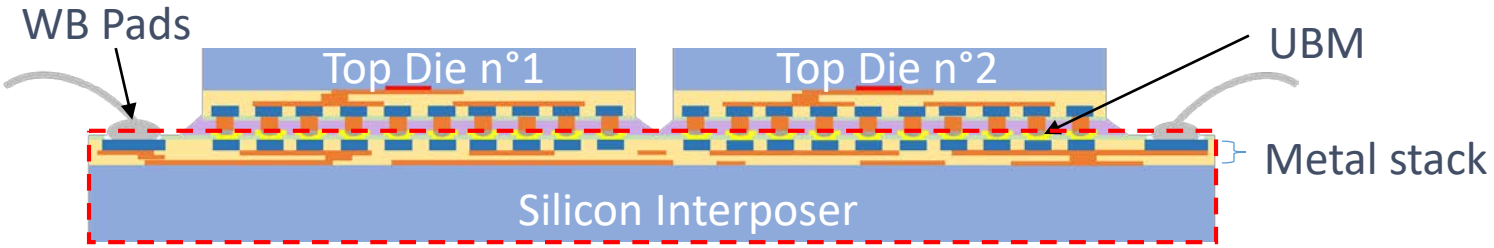
Silicon Interposer

Silicon Interposer using CMOS process platform:

Passive Interposer: Only the backend
Active Interposer: Front & Backend

Features:

- 4 layer metal stack (Thick last metal)
- Under Bump Metalization (Ni/Pd/Au)
- Wire-bond pads for connection to a PCB, or package



Pricing:

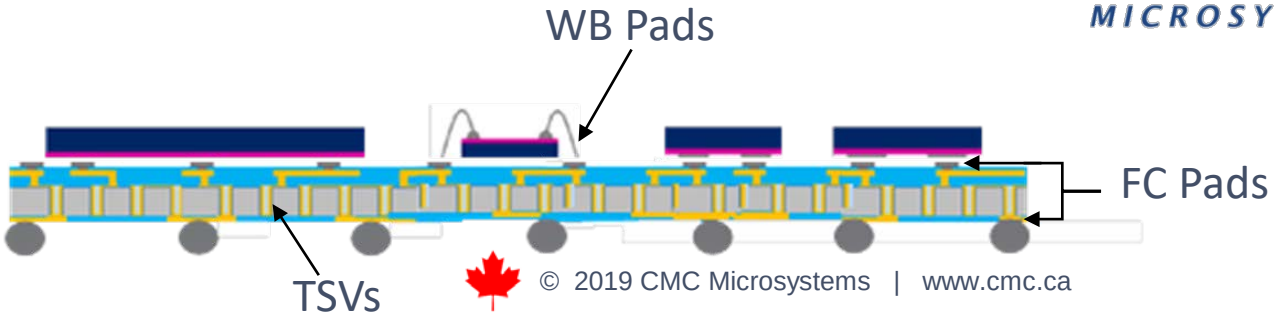
- Passive interposer: 40k€
- Active interposer: 50k€

Silicon Interposer

Multi-Technology Interposer in partnership with CMC:

Features:

- Standard tiles in multiples of 10mm x 10mm with 19x19 TSVs per tile
- 3 signal redistribution layers (two on top, one bottom)
- Under Bump Metallization (Ni/Pd/Au)
- Flip-chip & wire-bond pads
- Available PDK and tool support (Cadence & Tanner)



Pricing: TBD
Technology available in Q2

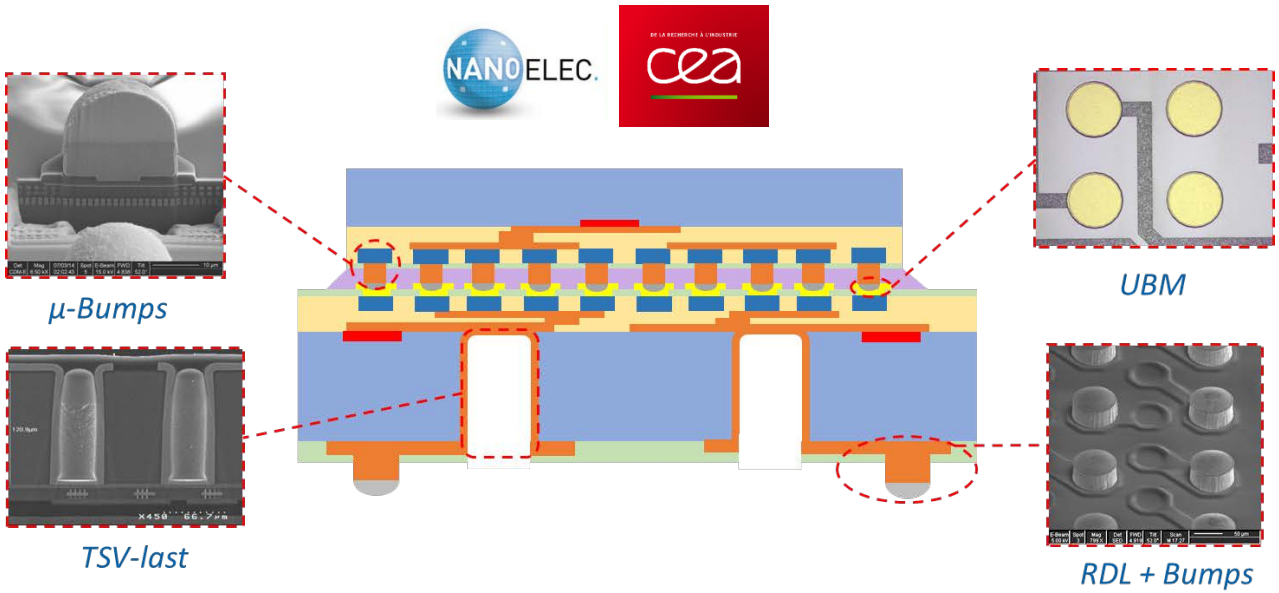
Contact: Peter Stokes
stokes@cmc.ca

OPEN 3D Post-process technology

3D interconnection integration at wafer level after standard MPW

Front-side modules:
- Cu-pillars (µ-Bumps)
- UBM

Back-side modules:
- TSV last
- RDL
- Bumps



Features:
- Available on any MPW and technology
- Specific add-on to the DK

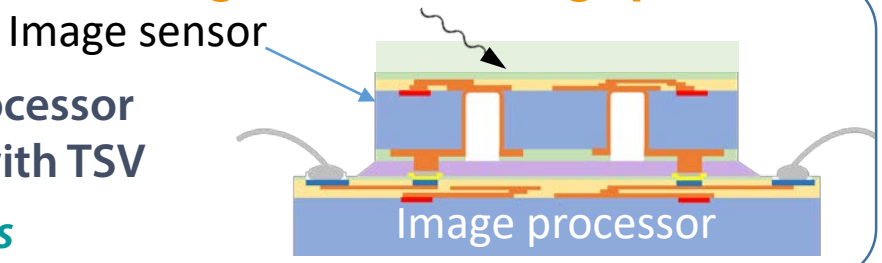
Pricing:
- Back-side post process: 55k€

OPEN 3D Application examples

Image sensor on image processor

- Small footprint
- 2 heterogeneous nodes for sensor and processor
- Top-die frontside access to light sensing with TSV

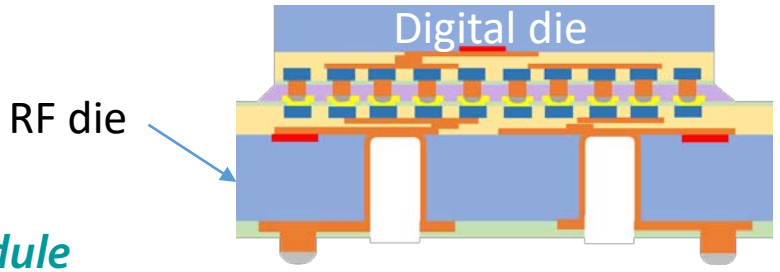
Application : Image sensor in embedded devices



Digital die on RF die

- High bandwidth between dies
- 2 heterogeneous nodes for :
  - High density digital die
  - Radio-frequency die

Application : Processor on RF communication module



CMOS die on Photonic IC

- Electronic die integration on Photonic IC

Application : Data center, HPC