Circuits Multi-Projets®

MPW Services Center for ICs, Photonics & MEMS
Prototyping & Low Volume Production

mycmp.fr

Grenoble - France
Flip-Chip Packaging

- Interconnects on silicon
- Custom substrate
  - μ-bumps/copper pillar
  - Solder Bumps
  - Gold stud bumps
- Flip-Chip assembly

Advanced Packaging

- Silicon Interposer
- OPEN 3D post process for 3D integration
In the frame of IRT Nanoelec, CEA LETI and CMP offer a **Micro Bumps post-process** *(or copper pillars)* realization manufactured at wafer-level.

**Features:**
- Pillar of copper (selective electro-deposition)
- Sn/Ag alloy capping
- Allows **very fine pitch** (down to 50µm)
- Improved electro migration VS solder bumps
- Assembly by reflow

**Prices & conditions:**
- As MPW: 40 dies delivered. Selected runs only. Available on the last MPW of the year & subject to a sufficient level of participation
- As a dedicated post-process: On any CMP runs (upon feasibility study).
CMP now offers a **Solder Bumps post-process** realization by an external subcontractor. This option is available for **any project** processed through CMP.

**Features:**
- Two steps process:
  - **Under Bump Metalization** electroless deposition (Ni/Au – Non-selective).
  - Solder ball individual placement (Sn/Ag/Cu alloy)
- Minimum pitch is 150 µm
- Assembly by **reflow**

**Prices & conditions:**
- Price is **design-dependent**: request a quotation.
- Electroless UBM is **strongly design-dependent**. For this reason, this service is offered for **R&D purposes only**, with a **best effort delivery from CMP**.
In partnership with ams, CMP offers a **Solder bump finishing** service realized at wafer level by ams on **any 0.35µm and 0.18µm** MPW run.

**Features:**

- ReDirection Layer deposition (selective) + UBM
- Solder sphere deposition & reflow
- I/O Pitch compatible with PCB assembly processes
- Assembly by reflow

**Prices & conditions:**

- Option is supported within ams hit kit upon request.
- 40 chips delivered
CMP now offers a **gold stud bumps** realization by an external subcontractor. This option is available for **any project** processed through CMP.

**Features:**
- Realized at **die-level** with wire-bonding equipment
- Ball bonded with **gold wire**, then cut
- **No RDL/UBM** required
- Assembly by **thermocompression/thermosonic/reflow**

**Prices & conditions:**
- 10 pieces delivered.
CMP can work with its subcontractors to deliver **ceramic or plastic custom substrates**. Advantages for the designers are:

- Die/Substrate compatibility verification before fabrication
- Technical information exchange with subcontractors ensured by CMP
- Optimizing turnover by coordinating the different links of the packaging chain.

**Prices & conditions:**
- Price depends on substrate specifications, you must request a quotation.
- This option is available on any CMP MPW runs.
CMP can work with its subcontractors to realize **Flip-Chip assembly**.

- Flip-Chip on *custom substrate* or directly on PCB
- **Choice of subcontractors/techniques** depends on:
  - Chip type
  - Interconnects type
  - Substrate type
- Various types of flip-chip technique: Reflow, thermocompression, thermosonic.
- Various options: Underfill, Encapsulation, SMD assembly, substrate backside balling...

**Request a feasibility study & quotation in the early stages of your project.**

Source: CEA-Leti/ STMicroelectronics
Flip-Chip Packaging

• Interconnects on silicon
• Flip-Chip assembly
• Custom substrate

Advanced Packaging

• Silicon Interposer
• OPEN 3D post process for 3D integration
CMP offers a service for two types of Silicon Interposer prototyping, in partnership with ams.

**Passive Interposer**: Only the back end, high density routing & passive integration.

**Active Interposer**: Active layer for CMOS integration, allowing a wider range of applications.

**Features**:
- 4 layer metal stack (Thick last metal) manufactured at ams foundry
- Under Bump Metalization (Ni/Pd/Au) post-processed by subcontractor
- Interposer includes wire-bond pads for connection to a PCB, or package
OPEN 3D post-process allows 3D interconnection integration on various technology nodes. Modules are integrated at wafer level after standard MPW.

**Front-side modules:**
- \(\mu\)-Bumps
- UBM

**Back-side modules:**
- TSV last
- RDL
- Bumps

**Prices & conditions:**
- **Specific add-on to the DK required for design**
- **As MPW** On ams C35B4, ST 28nm (frontside only), B9MW, 65nm and 55nm Available on the last MPW of the year & subject to a sufficient level of participation
- **As dedicated post-process:** Available on any MPW and technology (upon feasibility study)
### OPEN 3D Application examples

- **Small footprint**
- **2 heterogeneous nodes for sensor and processor**
- **Top-die frontside access to light sensing with TSV**

*Application: Image sensor in embedded devices*

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<tr>
<th><strong>Image sensor on image processor</strong></th>
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<td><img src="image2.png" alt="Image processor" /></td>
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<td><strong>Image sensor</strong></td>
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- **High bandwidth between dies**
- **2 heterogeneous nodes for:**
  - High density digital die
  - Radio-frequency die

*Application: Processor on RF communication module*

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<td><strong>Digital die</strong></td>
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- **Electronic die integration on Photonic IC**

*Application: Data center, HPC*

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<td><img src="image6.png" alt="Optic fiber" /></td>
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<td><img src="image7.png" alt="Si-Photonic IC" /></td>
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Post-Processed die combines two technologies, thus requiring a special consideration during design, verification and fabrication.

**3D Design kit**
- As an add-on to the foundry kit
- OPEN 3D post-process technology **integration to cadence**
- Specific **additional libraries** (Bumps, µ-bumps, TSV...)
- Specific calibre **die-level DRC deck**
- Specific **documentation** (DRM, tutorial ...)

**Assembly-level verifications**
- Run with calibre 3DSTACK
- Die-to-die **layout verification**
- Die-to-die **electrical connection verification**

**OPEN 3D post-process must be anticipated at an early stage, you must indicate it in the reservation form. CMP will take a special consideration to guide designers every step of the way for achieving their 3D projects.**
Conclusions

• **Flip-Chip** and **Advanced packaging** projects require **more consideration** than classical wire-bonding packaging projects.

• In the past three years, CMP has developed its **network, skills** and **tools** to offers its designers community a way to successfully achieve such projects.

• CMP can assist you with an **individual follow up** required for Flip-Chip and Advanced packaging projects.

• You must **plan ahead** these types of packaging, please contact CMP at **olivier.guiller@mycmp.fr** in the **early stages of your project**.
Thank you!