Circuits Multi-Projets®

MPW Services Center for ICs, Photonics & MEMS Prototyping & Low Volume Production

mycmp.fr

Grenoble - France
STMicroelectronics

Standard Technology offers at CMP in 2018
Deep Sub-Micron, SOI and SiGe Processes

http://mycmp.fr
STMicroelectronics Technology offers at CMP:

- **160nm CMOS: SOIBCD8s in 2018**
  - 160nm CMOS: BCD8SP
  - 130nm SiGe: BICMOS9MW & HCMOS9GP
  - 130nm SOI: H9SOI-FEM
  - 130nm HV-CMOS: HCMOS9A
  - 65nm CMOS: CMOS065LPGP
    - 55nm SiGe: BICMOS055
    - 28nm FDSOI: 28FDSOI
160nm SOIBCD8s: Bipolar-CMOS-DMOS Smart Power on SOI:

- 160nm Mixed Analog / Digital Bipolar-CMOS-DMOS 4LM on SOI
- Gate length: 180nm (drawn).
- 4 Cu metal layers, AlCu Thick Power M4.

- Operating voltages: 3.3V baseline, 1.8V optional: Digital & Analog.
- Medium Voltage Module Power MOS: 6V – 40V.
- High Voltage Module MOS: 70V – 200V.
- Dielectric Isolation on SOI.

- Analog + Digital + Power & HV on one chip.
  - High Voltage to drive external loads.
  - Analog block to interface « external world » to the digital systems.
  - Digital Core for signal processing.
- Memories SPRAM/ DPRAM / ROM available.

- 1 MPW run organised in 2018: 22nd February.
- Turnaround: 18 weeks to 24 weeks.
- Current supported version of Design Kits: 2.1

Applications: Automotive Sensor Interface ICs, 3D Ultrasound, MEMS & micro-mirror driver.
Deep Sub-micro 160nm: BCD8SP

- **160nm BCD8SP: Bipolar-CMOS-DMOS Smart Power:**
  - 160nm Mixed Analog / Digital Bipolar-CMOS-DMOS 4LM.
  - Gate length: 180nm (drawn).
  - 4 Cu metal layers, Thick Power M4, M4 Al optional.
  - Operating voltages: 1.8V - 5V : Digital & Analog.
  - Power devices: 10V - 18V - 27V - 42V - 60V.
  - Dual gate oxide process: 1.8V CMOS, 5V CMOS.
  - Analog + Digital + Power & HV on one chip.
    - High power transistor.
    - Low power digital and analog device.
  - Memories SPRAM/ DPRAM / ROM available free of charge on request.

- 3 MPW runs organised in 2018: **28th February, 24th April and 2nd October.**
- Turnaround: 18 weeks to 24 weeks
- Current supported version of Design Kits: **2.4.**

**Applications:** Power Management systems, DC-DC converter, Motor drivers, Printer.
Deep Sub-micro 130nm: H9-SOI-FEM

**130nm H9-SOI-FEM: Front-End Module:**

- **130nm mixed** A/D/RF CMOS SLP/M4TC (Thick Copper Metal Stack).
- Gate length: 130nm (drawn).
- Ultra-thick Cu top metal, 4 Cu metal layers.
- Body contacted CMOS.

- High Linearity MIM capacitor (2fF/mm²).
- 5.0V NLDMOS & PLDMOS.
- Standard cell libraries: IO cells, ESD kit.
- Floating body CMOS 5.0V NLDMOS.

- **Enabling 802.11 ac LNA integration**
  - High linearity requirement
  - Low NF at 5 GHz

- 200mm SOI wafers with high resistive (HR) substrate and Trap Rich SOI.

- 3 MPW runs organised in 2018: **21st March, 7th June and 29th October**.
- Turnaround: 16 weeks to 18 weeks.
- Current supported version of the design kits: **14.1**.

**Applications:** Radio receiver/transceiver, Cellular, Wifi, Automotive keyless systems.
130nm HCMOS9GP CMOS and BiCMOS9MW SiGe: General Purpose:

- 130nm mixed A/D/RF CMOS SLP/6LM (triple Well) HCMOS9GP.
- BICMOS9MW technology is using 130nm HCMOS9GP as base process.
- Power supply: 1.2V for core and 2.5V for IO.
- 6 Cu Metal layers, thick top metal layer.
- SiGe-C bipolar transistor (fT around 230GHz) in BiCMOS9MW.
- MIM capacitors.
- High performance and Medium voltage NPN bipolar transistor.
- Memories SPRAM/ DPRAM / ROM available free of charge on request.
- Lead-time for memory generation: 1 to 2 weeks.
- Standard cells libraries.
- Tutorial in development to ease the migration.

- 3 MPW runs organised in 2018: 14th February, 15th May and 14th November.
- Turnaround: 16 weeks to 18 weeks.
- Current supporter version of the Design kits: 2.9b in BiCMOS9MW.
- Current supporter version of the Design kits: 9.2 (RF option available) in HCMOS9GP.

Applications: General purpose Analog/Digital/ RF applications and Millimeter-Wave applications (frequencies up to 77GHz for automotive radars), WLAN, Optical communications.
130nm HCMOS9A HV-CMOS: Addon NVM with CEA-LETI

- Based on HCMOS9A 130nm mixed A/D/RF technology of STMicroelectronics, and with cooperation of CEA-LETI.
- CMP opens a new service for Non Volatile Memory integration in Q4, 2018.
- Standard cells Libraries: Core cells, PR, Analog and digital IO and NVM addon.
- LETI NVM design kit available in February/March 2018.

- Library name: Addon_NVM_Lib
  - Category Device: OxRam

1 MPW run organised in 2018: Q4 2018
Turnaround: 24 weeks to 30 weeks (dataprep/Front end ST and post-process CEA-LETI).
Current supported version of the design kits: 10.7.

Applications: For all applications requiring non-volatile memory.
130nm HCMOS9A HV-CMOS: Mixed Digital / Analog / Energy Management:

- 130nm mixed A/D/RF CMOS SLP/4LM (triple Well).
- Gate length: 130nm (drawn).
- 4 Cu metal layers, Thick M4.
- Low k inter-level dielectric.

- Operating voltages: 1V2 GO1, 4V8 for GO2, 20V for HV with DGO option.
- Specific Devices: N&P 20V Drift MOS with 85A gate oxide, MIM 5fF capacitor.
- Memories SPRAM / ROM available free of charge on request.
- Standard cells Libraries: Core cells, PR, Analog and digital IO.

1 MPW run organised in 2018: 25th November.
Turnaround: 16 weeks to 18 weeks.
Current supported version of the design kits: 10.7.

65nm CMOS65LPGP CMOS: Low Power General Purpose:

- 65nm mixed A/D/RF CMOS SLP/7LM (triple Well).
- Gate length: 65nm (drawn).
- 7 Cu metal layers.
- Dual gate oxide (1V for core and 2.5V for IO).

- Various Power supplies: 2.5V, 1.8V, 1.2V, 1V.
- MIM and Fringe MOM capacitors.
- Analog / RF capabilities.
- Multiple Vt transistor offering.

- High Density of integration: 800kgates/mm².
- Memories SPRAM/ DPRAM / ROM available free of charge on request.
- Standard cells libraries.
- RF kit available on request and subject to restriction.

3 MPW runs organised in 2018: 21st March, 7th June and 29th October.
Turnaround: 22 weeks to 26 weeks.
Current supported version of the design kits: 5.4.

Applications: General purpose, Analog/RF capabilities.
55nm BiCMOS055 SiGe: Low Power:

- 55nm mixed A/D/RF CMOS SLP/8LM (triple Well).
- Gate length: 55nm (drawn).
- 8 Cu metal layers, Ultra-thick Cu top metal.
- Low Power and General purpose MOS transistor.
- Dual gate oxide (1V for core, 2.5V for IO).
- MIM and Fringe MOM capacitors.
- Bipolar SiGe-C NPN transistors with Ft=320GHz.
- High density of integration: up to 970kgates/mm².
- Analog / RF capabilities.
- Various power supplies: 2.5V, 1.2V, 1V.
- Millimeter-wave inductor.

Applications: Optical, Wireless and High-Performance Analog Applications.
28nm FDSOI: Fully depleted Silicon On Insulator:

- 28nm mixed A/D/RF CMOS SLP/8LM (triple Well).
- Gate length: 28nm (drawn).
- 8 Cu metal layers (6 thin + 2 thick Cu top metal).
- Body biasing.
- Triple well Fully depleted SOI devices.
- IO supply voltage: 1.8 V using the IO oxide.
- Ultra low k inter-level dielectric.
- Low leakage (High density) SRAMS.
- Analog / RF capabilities.
- MIM and Fringe MOM capacitors.
- Standard cell libraries (more than 3Mgates/mm²).

2 MPW runs organised in 2018: 16th April, 5th November.
Turnaround: 24 weeks to 32 weeks.
Current supported version of the design kits: 2.9.

Applications: Low power and high performance applications
Standard Cells libraries included in STMicroelectronics Design kits:

- The content of libraries depends on each technology:

  - **CORE cells Libraries**:
    - CORE: General purpose core libraries.
    - CORX: Complementary core libraries (complex gates).
    - CLOCK: Buffer cells for clock tree synthesis.
    - PR: Place and route filler cells.
    - DP: Datapath leaf cells libraries.
    - HD: High density core libraries.

  - **IO cells Libraries**:
    - 1.8V, 2.5V, 3.3V IO pads:
      - 80µ, 65µ, 60µ, 50µ, 40µ and 30µ IO pads: Digital and Analog.
      - Staggered IO pads.
      - Flip-Chip pads.
      - Level Shifters, and compensation cells.
      - ESD.
STMicroelectronics IP blocks

- **RAMS and ROM block available through STMicroelectronics generators:**

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<th>Technology</th>
<th>SPREG</th>
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<th>DPREG</th>
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- **Flow for a request of block (1 or 2 weeks):**
  - Send to CMP type, number of words and number of bits.
  - Receive results of Cut explorer.
  - Send names of selected cuts.
  - Generation at STMicroelectronics, data preparation at CMP (reduced layouts).
  - Delivery of blocks. Data include layout, models for simulation, files for P&R.
## Supported CAD Tools by STMicroelectronics Design kits:

<table>
<thead>
<tr>
<th>IC</th>
<th>Electrical Simulation</th>
<th>Verification</th>
<th>Parasitic extraction</th>
<th>P&amp;R</th>
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From layout to chips: STMicroelectronics Design-kits
Reservation for MPW run one month before the CMP deadline is mandatory:

- Design transfer
  - Data checking (DRC)
  - Help for corrections (Report)
  - Data preparation (Sealring/Tiling)
  - Supports

- Wafers shipment

  12 to 28 weeks
  Depending on technologies

2 to 3 weeks
Report for corrections

Transfer validated designs

The global turnaround includes the data checking, verifications, supports and final data preparation done at CMP.

CMP annual users’ meeting - 25-Jan-18 - PARIS
The circuits must be sent at CMP by FTP:
- You must send your circuit without sealring and without tiling.
- You must run DRCs on the gds2 file before sending it. DRC must be clean except low densities outside exclusion area.

DRC is free of fatal error

Sealring generation

- Addition of the sealring
- Addition of logos
- Addition of foundry cells
- Move to origin

Dummies generation

- Verification of generated dummies
- Final DRC
- Verification of densities
- Report to the user if necessary
- Preparation of final database
- Shipment to ST
Thank you!