Performances of recent outstanding 28FDSOI circuits and systems taped out through the CMP services

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Fully depleted Silicon-on-Insulator (FD-SOI)

- Power and energy efficiency
- Analog performance for mixed signal and RF design
- Robustness for mission critical applications

FD-SOI is unmatched for cost-sensitive markets requiring digital and Mixed Signal SoC integration and performance
Addressing Power Sensitive Markets

FD-SOI

FinFet

High-end Servers

Laptops

Tablet PC

Networking Infrastructure

Smartphone

Internet of Things, Wearables

Automotive

Ultimate Digital Density

Ultimate Digital / Analog & Mixed-Signal / RF Integration
ST 28nm FD-SOI Transistor Flavors

Low VT (LVT) CMOS in FD-SOI; flipped-well

Regular VT (RVT) CMOS in FD-SOI
ST 28nm FD-SOI makes analog/RF/HS designer’s life easier

- **Improved Analog Performance**
  - Speed increase in all analog blocks
  - Higher gain for a given current density

- **Improved Noise**
  - Lower gate and parasitic capacitance
  - Lower noise variability

- **Efficient Short Devices**
  - Better matching for short devices and efficient design with L>L_{\text{min}}

- **Very large $V_T$ tuning range**
  - Analog parameters wide range tuning via a new independent “tuning knob” (back-gate)

- **High performance frequency behavior**
  - $f_T/f_{\text{max}} >300\text{GHz}$ for LVTNMOS and high performance passives enabling RF/mmW/HS integration with technology margin

- Higher bandwidth
- Lower power
- Smaller designs
- Improved design margins wrt PVT variations
- Novel flexible design architectures
Advantages in Analog Design

Efficient Short Devices

- Efficient use of short devices:
  - High analogue gain @ Low L
  - Low Vt mismatch (Avt ~ 2mV.µm)
- Performance example:
  - A 1µm/100nm device has a DC gain of 80 & a σVt of only 6mV

Improved Analog Perf.

- Higher Gm for a given current density
- Lower gate capacitance
- Higher achievable bandwidth or lower power for a given bandwidth

Improved Noise

- For NLVT MOS 1µm/120nm @ 1μA drain current, get 1.5dB lower 1/f noise in FDSOI
Advantages in Analog Design-II

- Flip-well devices:
  - Large Forward Body Bias (FBB) range
  - Negligible control current

- Use back-gate as « VT tuning knob »:
  - Unprecedented ~250mV of tuning range for FD-SOI vs.
  - ~ 10's mV in any bulk

**Very large $V_T$ tuning range by FBB**

![Graph showing $V_T$ vs. Forward body bias (V) for Bulk and FD-SOI](image)

- ST 28nm LVT NMOS (typical)

- NMOS and PMOS devices

- Forward body bias [V] vs. $V_T$ [mV]

- P-Sub
- Bulk
- N-Well
- P-Well
- BOX
- VBBN
- VBBP
- P-Sub
- FBB

- +3V
- -3V
- 0V
- P-sub
Advantages in RF/mmW Design

Active devices high frequency performance

- For RF operation frequency:
  - Work with L = 100nm
  - MAG = 12dB @10GHz
  - NFmin ~ 0.5dB @ 10GHz
  - Work @ current density: 125 µA/µm

- For mmW operation frequency (intrinsic models):
  - Work @ Lmin
  - MAG = 12dB @60GHz
  - NFmin ~ 1.3dB @ 60GHz
  - Work @ current density: 200 µA/µm ➔ 33% less power than in 28LP bulk

Performant passive devices

- Few passive devices examples:
  - Inductor L=0.5nH Q=18 @10GHz, 8ML
  - Varactor C=50fF Q=20 @20GHz
  - Tline: 0.8dB/mm @60GHz Zc=50 Ohm, 8ML
Advantages in Mixed Signal Design

- Tighter process corners and less random mismatch than competing processes
- Benefits:
  - Simpler design process, shorter design cycle
  - Improved yield or improved performance at given yield

<table>
<thead>
<tr>
<th>Variability</th>
<th>Switch performance</th>
<th>Lower capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vth (mV)</td>
<td>Improved gate control allows smaller VTH</td>
<td></td>
</tr>
<tr>
<td>28FDSOI</td>
<td>Backgate bias allows for VTH reduction by tuning</td>
<td></td>
</tr>
<tr>
<td>28lp bulk</td>
<td>Results is an unprecedented quality of analog switches</td>
<td></td>
</tr>
<tr>
<td>Gate length (m)</td>
<td>Compounding benefits: smaller R -&gt; smaller switch -&gt; compact layout -&gt; lower parasitics -&gt; even smaller switch</td>
<td></td>
</tr>
</tbody>
</table>

Key for high performance data converters and other Switched-Cap. Circuits

- Lower junction capacitance makes a substantial difference in high-speed circuits
  - Drastic reduction of self-loading in gain stages
  - Drastic reduction of switch self-loading
- Two-fold benefit:
  - Leads to incremental improvements
  - Allows the designer to use circuit architectures that would be infeasible/inefficient in bulk technologies
Forward Body Biasing: An extremely powerful and flexible concept in FD-SOI

- Performance boost
- Reduce power consumption at a given performance requirement
- Process compensation reducing the margins to be taken at design
- Seamless inclusion in the EDA flow

Comparatively easy to implement
If you’ve ever done DVFS you’ll have no difficulty with Body Biasing
Body Bias Advantages

- Boost performances
- Enable area reduction
- Improve power efficiency
- Reduce process dispersion
- Enable leakage reduction
- Allow compensation techniques
Process Compensation Through FBB

- Process compensation through FBB allows
  - Masking SS-FF process spread
  - Recovering +17% speed in 28nm FD-SOI, at no dynamic power expense
Design examples in 28nm FD-SOI
- from building blocks to SoC's
A Digital Delay Line with Coarse/Fine tuning through gate/body biasing in 28FDSOI

- Novel low power design architectures for 60GHz receivers enabled by FDSOI: DFE with un-clocked delay feedback, search minimum delay spread at 2GS/s data rate
  - Total delay >10ns
  - Granular delay < 500ps

- FDSOI specific unity delay cell (thyristor revisited):
  - Body bias control for rising/falling edge delay fine tuning
  - Gate control for coarse delay tuning
  - Complementary input scheme for reduced power consumption

- State of the art results: ultra wide range linear control, fs/mV sensitivity and energy efficiency [I. Sourikopoulos et al., ESSCIRC2016]
The oscillation frequency depends on:

- The electrical Tline parameters
- The transistor inverting properties around Fosc (Fmax)
- The highest Fosc topology proposed so far in a 28nm node

Phase noise optimization through body bias tuning
Oscillation frequency measurements, histogram over 8 locations on a wafer:

- <0.1% variation simulation vs measurements ➔ Very small on wafer dispersion

Simulation: \( f_{osc} = 134.14 \text{GHz} \)
Theory: \( f_{osc} = 134.2 \text{GHz} \)

Oscillation frequency (Fosc)
A 128 kb Single-Bitline 8.4 fJ/bit 90MHz at 0.3V 7T Sense-Amplifier-less SRAM in 28nm FD-SOI

- 7T SRAM architecture with new: single clock cycle and low area booster, decoding scheme and read architecture (no sense-amplifier)
- Energy efficiency achieved by keeping the storage-elements at ULV, whereas critical nodes are boosted
- Intensive body biasing design
- State of the art performance:
  - 90MHz read speed at 300mV, dissipating 8.4 fJ/bit-access
  - the minimum operating voltage is 240mV
  - the retention voltage is 200mV

[B. Mohammadi et al., ESSCIRC2016]
First proof-of-concept pitch-matched fully-digital subarray beamformer IC for 3D ultrasound
  • Highest per-channel SNR with ~7x area reduction

**FDSOI Technology Enabler:**
  • High integration density
  • Immune to latch-up allow the use of slewing-based amplifier using minimum length cascaded inverters
  • Low $V_{th}$ devices provide area-efficient low $R_{on}$ switches

* [M-C. Chen et al., ISSCC2017 and JSSC Dec2017]
SleepTalker - 28nm FDSOI ULV WSN Transmitter: RF-mixed signal-digital SoC

- IR-UWB BPSK and BPM RF transmitter operated at 0.55V
- IEEE 802.15.4a compliant
- 3.5 – 4.0 – 4.5GHz channels reconfiguration
- Configurable Data Rate: 0.11, 0.85, 1.7, 6.81, 27.24Mb/s
- RF SoC: digital and RF transmit path, frequency synthetizer, DC-DC (1.2V to 0.55V) and Body Bias Generator (up to +/-1.8V, for variable output voltage)
- **SoC architecture innovation enabled by FDSOI:**
  - Extremely low power PLL-free architecture with aggressive duty cycling, compensated by on chip adaptive FBB for Local Oscillator tuning and trimming upon the requested transmit frequency
  - Digital Power Amplifier with programmable pulse shaping enabled by body biasing control, meeting FCC spectral regulation for all channels
  - High speed – ultra low voltage digital implementation enabled by FBB
- Record energy efficiency improving by 16 the State of the Art (Tx: 14pJ/bit, SoC: 24pJ/bit)

[G. de Streel, D. Bol et al., VLSI2016 and JSSC2017]
A 128x8 Massive MIMO Precoder-Detector in 28FDSOI

- Flexible solution wrt to classical 4x4 MIMO implementations, improves by 12dB array and 2X spatial multiplexing gains
- Hardware reuse, clock-gating, body biasing
- Uses FBB and RBB for performance-power trade-off and fine tuning of PVT
- The downlink pre-coder QRD unit has the highest reported energy efficiency @ lowest reported area cost
- Uplink detector shows the highest reported energy efficiency and area efficiency detection

[H. Prabhu et al., ISSCC2017]
ENVISION: A 0.26-to-10TOPS/W Subword-Parallel Dynamic-Voltage-Accuracy-Frequency-Scalable Convolutional Neural Network Processor in 28nm FDSOI

Energy efficient FDSOI-enabled processor for deep neural network inference

- Local processing in connected objects
- Complete processor with state-of-the-art energy efficiency
  - Up to 10TOPs/Watt
- Approximate computing techniques exploiting body biasing
  - Scaling 2-16bit accuracy, for >10x efficiency improvement with different bias settings for each accuracy level
- 18% energy efficiency gains due to body bias

![Throughput vs. Energy Efficiency](image)

<table>
<thead>
<tr>
<th>Technology</th>
<th>ISSCC '16</th>
<th>VLSI '16</th>
<th>This work N = 1, 2 or 4</th>
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<tbody>
<tr>
<td>Technology</td>
<td>65nm LP</td>
<td>40nm LP</td>
<td>28nm FDSOI</td>
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<tr>
<td>V @ fnom</td>
<td>200MHz</td>
<td>200MHz</td>
<td>200MHz</td>
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<tr>
<td>Peak GOPS</td>
<td>1V</td>
<td>1V</td>
<td>1V</td>
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<tr>
<td>fnom</td>
<td>67</td>
<td>1.1V</td>
<td>N x 102</td>
</tr>
<tr>
<td>Anet CONV</td>
<td>278mW @ 35fps</td>
<td>76mW @ 47fps</td>
<td>44mW @ 47fps</td>
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<tr>
<td>VGG CONV</td>
<td>-</td>
<td>-</td>
<td>26mW @ 17fps</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>@ GOPS, nom</td>
<td>Min. Eff.</td>
<td>Max. Eff.</td>
</tr>
<tr>
<td>235-332 (1.5x)</td>
<td>0.17 TOPS/W</td>
<td>0.25 TOPS/W</td>
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<tr>
<td>@ 46 GOPS</td>
<td>0.27 TOPS/W</td>
<td>1x16b</td>
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<tr>
<td>35-300 (8.5x)</td>
<td>0.25 TOPS/W</td>
<td>2x8b</td>
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<tr>
<td>@ 80 GOPS</td>
<td>0.27 TOPS/W</td>
<td>4x4b</td>
<td></td>
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<tr>
<td>7.5-300 (40x)</td>
<td>2.60 TOPS/W</td>
<td>4x3-4b</td>
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<tr>
<td>@ 76 GOPS</td>
<td>0.25 TOPS/W</td>
<td>30-60% Sparse</td>
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<tr>
<td>10.0 TOPS/W</td>
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[B. Moons et al., ISSCC2017]
Fine-Grained AVS in 28nm FDSOI Processor SoC

- Energy-efficient FDSOI-enabled processor SoC featuring:
  - Intensive deployment of body biasing techniques
  - Integrated voltage regulation
    - 82-89% system efficiency with adaptive clocking
  - Fully-featured processor (RISC-V Rocket Processor)
    - 41.8 DP GFLOPS/W with integrated regulators
  - Integrated power management
    - Low-overhead power estimation
    - Programmable PMU
  - Sub-μs adaptive voltage scaling (AVS)
    - Up to 40% energy savings
  - Compact implementation:
    - Core area: 1.07mm²
    - 568k Std Cells
  - Boots Linux

[B. Keller et al., ESSCIRC2016 and JSSC2017]
Conclusion
Takeaways for Analog/RF/mixed-signal body biasing

- Unprecedented very wide $V_T$ tuning range of ~250mV for FDSOI vs ~10mV for bulk
- New “tuning knob” with no parasitic effects on the signal path (control under the BOX)
- Enhanced switches performances for all type of mixed-signal circuits
- Efficient revisited tuning/trimming strategies:
  - Process/Temperature compensation
  - Circuit reconfiguration
- Flexible and energy saving SoC solutions
- Simpler circuits revisit State of the Art
FD-SOI will Enable the Ultimate Integration for Tomorrow’s Connected World

- Ultra low voltage operations with high performance.
- Easy and efficient analog integration (ADC/DACs, RF, LDOs, ...)
- FBB for dynamic power/leakage/frequency tuning
- Excellent reliability and soft-error performances
- Performant Ft / Fmax, Performant passive devices
- Improved noise, Lower parasitic capacitances
- Adapt power consumption to load
- Performance and power efficiency

Network infrastructure
The Internet of Things

Enterprise & Cloud Datacenter
Core Network
Backhaul Mobile Network
Access Network
Radio Access Network
.... and in BiCMOS55
B55 Design of Low-Power Active Tags for Operation with 77-81 GHz FMCW Radar

[M.S. Dadash et al., IMS2017 and MTT2017]

- 1st low-power W-band active-tag in 55nm SiGe BiCMOS
- 19dB gain, 9GHz BW, and NF<sub>50</sub> < 9 dB
- Wake-up function with -62dB sensitivity
- 25/10.8mW in active/stand-by mode from 2.5/1.8 V supplies.
A Compact 130 GHz Fully-Packaged Point-to-Point Wireless System with 3D-Printed 26dBi Lens Antenna Achieving 12.5Gbps at 1.55 pJ/bit/meter

OOK Transceiver Performance:
- A low-cost, energy efficient, high-capacity, scalable, easy-to-deploy, and fully-packaged point-to-point wireless link using OOK modulation.
- Measurement results verify 12.5Gbps OOK data transmission over 5m.
- Energy/bit/range FoM is improved >40x compared to the state-of-the-art.
- Enabled by high gain antenna, efficient and low-cost packaging, and efficient TRX design.

B55 Technology Enablers:
- High integration density.
- Combined RF/baseband solutions using BiCMOS technology.
- High $f_t/f_{max}$ enabling high-frequency operation.
- High output power enabled by high performance and efficient BJTs.

[Ref: Nemat Dolatsha, et al. ISSCC 2017]
ST and the CMP

- A continued collaboration since almost 30 years
  - Win-win operation
  - Recognized by ST as best service unit for SME and research institutes
  - Supports ST’s customers for small volume business
  - Creating ecosystem in advanced More Moore and More Than Moore Silicon technologies

- The CMP: a professionnal team dedicated to their Users’ best experience in designing and prototyping IC’s