STMicroelectronics

Standard Technology offers at CMP in 2017
Deep Sub-Micron, SOI and SiGe Processes

http://cmp.imag.fr
STMicroelectronics Technology offers at CMP:

- 160nm CMOS: BCD8SP
- 160nm CMOS: SOIBCD8s **New**
- 130nm CMOS: HCMOS9GP
- 130nm SiGe: BICMOS9MW
- 130nm SOI: H9SOI-FEM
- 130nm HV-CMOS: HCMOS9A

65nm CMOS: CMOS065LPGP

55nm SiGe: BICMOS055

1994 at CMP

AMS 0.8μm
18k gates/mm²
1.2k gates/mm²

AMS 0.6μm
3k gates/mm²

ST 0.25μm
180k gates/mm²
80k gates/mm²

ST 0.35μm
50k gates/mm²

ST 0.18μm
35k gates/mm²

ST 130nm
180k gates/mm²

ST 90nm
400k gates/mm²

ST 65nm
800k gates/mm²

ST 55nm
970k gates/mm²

ST 28nm
3M gates/mm²

2017 at CMP

1/1000 x gate delay (from ns to ps).

1/1000 x power consumption (from µW/MHz to pW/MHz).

1300 x density integration.
Deep Sub-micro 160nm: BCD8SP

- **160nm BCD8SP: Bipolar-CMOS-DMOS Smart Power:**
  - 160nm Mixed Analog / Digital Bipolar-CMOS-DMOS 4LM.
  - Gate length: 160nm (drawn).
  - 4 Cu metal layers, Thick Power M4.
  - Operating voltages: 1.8V - 5V: Digital & Analog.
  - 10V – 65V: Power MOS.
  - Analog + Digital + Power & HV on one chip.
    - High Voltage to drive external loads.
    - Analog block to interface « external world » to the digital systems.
    - Digital Core for signal processing.
  - Memories SPRAM/ DPRAM / ROM available free of charge on request.
  - Lead-time for memory generation: 1 to 2 weeks.

- **2 MPW runs organised in 2017: 10th March and 10th September.**
- **Starting Price: 2800€/mm² for 25 samples.**
- **Turnaround: 18 weeks.**
- **Current supported version of Design Kits : 2.0a.**
- **2 Centers received the design rules and design kits.**

**Applications:** Hard Disk Drivers, Power Combo, Motor Drivers, DC-DC converter, Power Management.
160nm SOIBC8D8s: Bipolar-CMOS-DMOS Smart Power on SOI:

- **160nm Mixed** Analog / Digital Bipolar-CMOS-DMOS 4LM on SOI
- Gate length: 160nm (drawn).
- 4 Cu metal layers, Thick Power M4.
- Operating voltages: 1.8V (optional) - 3.3V (baseline) : Digital & Analog.
  - 6V – 40V: Power MOS
  - 70V – 200V: High Voltage MOS
- Analog + Digital + Power & HV on one chip.
  - High Voltage to drive external loads.
  - Analog block to interface « external world » to the digital systems.
  - Digital Core for signal processing.
- Memories SPRAM/ DPRAM / ROM available free of charge on request.
- **Dielectric Isolation on SOI**
  - MPW runs organised in 2017: 29 September 2017
  - Starting Price: 2800€/mm² for 25 samples (to be confirmed)
  - Turnaround: 18 weeks
  - Current supported version of Design Kits : TBD

**Applications:** Audio Amplifier, Sensor Interface ICs, 3D Ultrasound.
SOI Isolation versus Junction Isolation

**Advantages**
- Parasitic bipolars elimination
- Reduced isolation distance
- Below Ground capability
- EMI robustness

**Drawbacks**
- High cost of substrate
- Parasitic capacitance
- Thermal effect

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**SOI BCD is convenient or even mandatory in case of:**

- Ultrasound Probe ASIC
- μ-mirror driver
- Amoled Power Supply
- High Voltage
- Noise Immunity
- Below Ground pins
- Low Consumption
- Car Radio – Full digital amplifier
- Automotive Sensor ASIC Airbag
### Device Portfolio

#### Low Voltage
- 1.8V CMOS (3.5nm oxide)
- 3.3V CMOS (7nm oxide)

#### Medium Voltage
- N-DRIFT on GOX=7nm 6V, 20V, 40V
- P-DRIFT on GOX=7nm 6V, 40V

#### High Voltage
- N-DRIFT on GOX=7nm 70V, 100V, 140V, 200V
- P-DRIFT on GOX=7nm 70V, 100V, 140V, 200V

#### Diodes
- 5V Zener
- p+/Nwell, p+/Nwell3V3
- n+/Pwell, n+/Pwell3V3
- HV Fast Diodes 100V/200V

#### Capacitors
- 1.8V/3.3V poly P+ on pwell
- 1.8V/3.3V poly N+ on cpcimp (pwell)
- 5V poly-poly HL
- 100/200V MOM
- 30V MOM interdigitated

#### Resistors
- Poly resistors, including HIPO resistor (1kOhm and 6kOhm/sq)
- Diffused resistors
- Thin film resistor

#### Bipolar
- 5V NPN
- 5V NPN w/ CPCIMP
- 3.3V PNP

#### Trimming
- OTP Antifuse on 7nm GOX
130nm HCMOS9GP CMOS and BiCMOS9MW SiGe: General Purpose:

- 130nm mixed A/D/RF CMOS SLP/6LM (triple Well) HCMOS9GP.
- BICMOS9MW technology is using 130nm HCMOS9GP as base process.
- Gate length: 130nm (drawn).

- 6 Cu Metal layers.
- SiGe-C bipolar transistor (fT around 230GHz) in BiCMOS9MW.

- High performance and Medium voltage NPN bipolar transistor.

- Memories SPRAM/ DPRAM / ROM available free of charge on request.
- Lead-time for memory generation: 1 to 2 weeks.

3 MPW runs organised in 2017: 23rd February, 12th July, 22nd November.
Starting Price: 2500€/mm² (H9GP) and 3100mm² (BiCMOS9PW) for 25 samples.
Turnaround: 18 weeks.
Current supporter version of the Design kits: 9.2 (RF option available) in HCMOS9GP.
Current supporter version of the Design kits: 2.7 in BiCMOS9MW.
339 Centers received the design rules and design kits.
18 circuits manufactured in 2016 (33 circuits in 2015).

Applications: General purpose Analog/Digital/ RF applications and Millimeter-Wave applications (frequencies up to 77GHz for automotive radars), WLAN, Optical communications.
Deep Sub-micro 130nm: H9-SOI-FEM

- **130nm H9-SOI-FEM: Front-End Module:**
  - 130nm mixed A/D/RF CMOS SLP/M4TC (Thick Copper Metal Stack).
  - Gate length: 130nm (drawn).
  - 4 Cu metal layers, 1 thick copper.
  - Power supply: 1.2 V.

  - High Linearity MIM capacitor (2fF/mm²).
  - 5.0V NLDMOS & PLDMOS.
  - RAMS: No available RAM/ROM.

- 200mm SOI wafers with high resistive (HR) substrate and Trap Rich SOI.

3 MPW runs organised in 2017: 19th February, 6 July and 16th November.
Starting Price: 2400€/mm² for 25 samples.
Turnaround: 12 weeks.
Current supported version of the design kits: 14.1.
23 Centers received the design rules and design kits.
9 circuits manufactured in 2016 (3 circuits in 2015).

**Applications:** Radio receiver/transceiver, Cellular, Wifi, Automotive keyless systems.
130nm HCMOS9A HV-CMOS: Mixed Digital / Analog / Energy Management:

- 130nm mixed A/D/RF CMOS SLP/4LM (triple Well).
- Gate length: 130nm (drawn).
- 4 Cu metal layers, Thick M4.
- Low k inter-level dielectric.
- Operating voltages: 1V2 GO1, 4V8 for GO2, 20V for HV with DGO option.
- Single Gate Oxide option also qualified: No GO1 1V2 CMOS.
- Specific Devices: N&P 20V Drift MOS with 85A gate oxide, MIM 5fF capacitor.
- Memories SPRAM / ROM available free of charge on request.
- Lead-time for memory generation: 1 to 2 weeks.

1 MPW run organised in 2017: 2sd November.
Starting Price: 2500€/mm² for 25 samples.
Turnaround: 12 weeks.
Current supported version of the design kits: 10.7.
21 Centers received the design rules and design kits.
No circuit manufactured in 2016 (2 circuits in 2015).

Applications: Implantable devices, Robots/drones, Energy harvesting applications, Sensors wireless, Connected devices/Internet of thing(cell phones), Autonomous systems.
Deep Sub-micro 65nm: CMOS65LPGP

- **65nm CMOS65LPGP CMOS: Low Power General Purpose:**
  - 65nm mixed A/D/RF CMOS SLP/7LM (triple Well).
  - Gate length: 65nm (drawn).
  - 7 Cu metal layers.
  - Low k inter-level dielectric (k=2,9).
  - Power supply: 2.5V, 1.8V, 1.2V, 1V.
  - Multiple Vt transistor offering.
  - High Density of integration: 800kgates/mm².
  - Memories SPRAM/ DPRAM / ROM available free of charge on request.
  - Lead-time for memory generation: 1 to 2 weeks.

3 MPW runs organised in 2017: 9th March, 22th June and 19th October.
Starting Price: 6500€/mm² for 25 samples.
Turnaround: 22 weeks.
Current supported version of the design kits: 5.3.7 (RF option available).
377 Centers received the design rules and design kits.
18 circuits manufactured in 2016 (68 circuits in 2015).

**Applications:** General purpose, Analog/RF capabilities.
Deep Sub-micro 55nm: BiCMOS055

- **55nm BiCMOS055 SiGe: Low Power:**
  - 55nm mixed A/D/RF CMOS SLP/8LM (triple Well).
  - Gate length: 55nm (drawn).
  - 8 Cu metal layers.
  - Power supply: 1.2V and 2.5V for core.
  - 1.8V, 2.5V and 3.3V for IOs.
  - **Bipolar SiGe-C NPN transistors:**
    - High Speed NPN.
    - Medium Voltage NPN.
    - High Voltage NPN.
  - Millimiter-wave inductor.
  - 2.5V Drift NMOS and PMOS.

3 MPW runs organised in 2017: 21st March, 8th June and 27th October.

- **Starting Price:** 7900€/mm² for 25 samples.
- **4mm² block price:** 25,6k€ for 25 samples.
- Turnaround: 24 weeks.
- **Current supported version of the design kits:** 2.4

27 Centers received the design rules and design kits.
9 circuits manufactured in 2016.

**Applications:** Optical, Wireless and High-Performance Analog Applications.
Deep Sub-micro 28nm: FDSOI28

- **28nm FDSOI: Fully depleted Silicon On Insulator:**
  - 28nm mixed A/D/RF CMOS SLP/10LM (triple Well).
  - Gate length: 28nm (drawn).
  - 8 Cu metal layers (6 thin + 2 thick).
  - Low leakage (High Density) SRAM using Low Power core oxide.
  - IO supply voltage: 1.8 V using the IO oxide.
  - Ultra low k inter-level dielectric.
  - RAMS: RAMS and ROM available.
  - Lead-time for memory generation: 1 to 2 weeks.
  - Process options:
    - MIM: Metal-Insulator-Metal capacitance.
    - OTP (anti-Fuse): Capacitance + Drift MOS transistor.

3 MPW runs organised in 2017: 30th January, 15th April, to be announced.
Starting price: 12500€/mm² for 25 samples.
4mm² block price: 39.4k€ for 25 samples.
Turnaround: 28 weeks.
**Current supported version of the design kits:** 2.7.a.
214 Centers received the design rules and design kits.
46 circuits manufactured in 2016 (61 circuits in 2015).

**Applications:** Low power and high performance applications
10 metal layers (10ML) process flavor with MIM capacitor are standard options on the 2 first MPW runs in 2017. These options are still available for the following MPW but, specific quotation will apply.
Standard Cells libraries included in STMicroelectronics Design kits:

- **CORE cells Libraries:**
  - CORE: General purpose core libraries.
  - CORX: Complementary core libraries (complex gates).
  - CLOCK: Buffer cells for clock tree synthesis.
  - PR: Place and route filler cells.
  - DP: Datapath leaf cells libraries.
  - HD: High density core libraries.

- **IO cells Libraries:**
  - 1.8V, 2.5V, 3.3V IO pads:
    - 80μ, 65μ, 60μ, 50μ 40μ and 30μ IO pads: Digital and Analog.
    - Staggered IO pads.
    - Flip-Chip pads.
    - Level Shifters, and compensation cells.
    - ESD.
STMicroelectronics IP blocks

- **RAMS and ROM block** available through STMicroelectronics generators:

<table>
<thead>
<tr>
<th>Technology</th>
<th>SPREG</th>
<th>SPRAM</th>
<th>DPREG</th>
<th>DPRAM</th>
<th>ROM</th>
<th>MPSRAM</th>
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<tbody>
<tr>
<td>BCD8SP</td>
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<tr>
<td>HCMOS9GP</td>
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<tr>
<td>BICMOS9MW</td>
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<td>CMOS28FDSOI</td>
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<td>Yes</td>
<td>Yes</td>
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</table>

- **Flow for a request of block** (1 or 2 weeks):
  - Send to CMP type, number of words and number of bits.
  - Receive results of Cut explorer.
  - Send names of selected cuts.
  - Generation at STMicroelectronics, data preparation at CMP (reduced layouts).
  - Delivery of blocks. Data include layout, models for simulation, files for P&R.
**Supported CAD Tools by STMicroelectronics Design kits:**

<table>
<thead>
<tr>
<th>IC</th>
<th>Electrical Simulation</th>
<th>Verification</th>
<th>Parasitic extraction</th>
<th>P&amp;R</th>
</tr>
</thead>
<tbody>
<tr>
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<td>CD 5.1.41</td>
<td>OA 6.1.5</td>
<td>Spectre (DS)</td>
<td>Calibre (MGC)</td>
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<td>x</td>
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<tr>
<td>BICMOS9MW</td>
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<td>x</td>
<td>x</td>
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<tr>
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<td>x</td>
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<td>CMOS065</td>
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<td>x</td>
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<td>BICMOS55</td>
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<tr>
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<tr>
<td>BCD8sP</td>
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<td>x</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>
Submission cycle for CMP users

- Research Laboratories
- Education & Universities
- Companies, Startup

- Design transfer
- Wafers shipment

Users

- Data checking (DRC)
- Help for corrections (Report)
- Data preparation (Sealring/Tiling)
- Supports

Validated Transfer designs

Report for corrections

- 2 to 3 weeks

Process

<table>
<thead>
<tr>
<th></th>
<th>0.35 CMOS</th>
<th>130nm CMOS</th>
<th>65nm CMOS</th>
<th>55nm CMOS</th>
<th>28nm CMOS</th>
<th>28nm FDSOI</th>
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<tbody>
<tr>
<td>Nbr. Of DRC Rule Checks</td>
<td>400</td>
<td>750</td>
<td>1650</td>
<td>2770</td>
<td>4650</td>
<td>5250</td>
</tr>
</tbody>
</table>

12 to 28 weeks Depending on technologies

CMP annual users’ meeting, 26-Jan-17, PARIS
The circuits must be sent at CMP by FTP:
- You must send your circuit without sealring and without tiling.
- You must run DRCs on the gds2 file before sending it. DRC must be clean except low densities outside exclusion area.

DRC is free of fatal error

Sealring generation

Dummies generation

- Replacement of ST standard cells
- Verification of ST standard cells used
- Data checking + DRC
- Help for corrections (Report)
- Supports

- Addition of the sealring
- Addition of logos
- Addition of fondry cells
- Move to origin

- Verification of generated dummies
- Final DRC
- Verification of densities
- Report to the user if necessary
- Preparation of final database
- Shipment to ST

CMP annual users’ meeting, 26-Jan-17, PARIS
Thank you!