OXRAM MEMORIES:
A DISRUPTIVE TECHNOLOGY FOR DISRUPTIVE DESIGNS

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• Leti & NVM

• OxRAM:
  • Disruptive Technology
  • Disruptive Designs

• MAD200 offer to explore OxRAM memories

• Conclusion
TOP 10 INSTITUTIONS|2015 RANKINGS

1 – CEA / FRANCE
2 - Fraunhofer Society / GERMANY
3 - Japan Science & Technology Agency / JAPAN
4 - U.S. Dept of Health & Human Services / USA
5 – CNRS / FRANCE
6 – KIST / SOUTH KOREA
7 – AIST / JAPAN
8 - U.S. Department of Energy / USA
9 – A*STAR / SINGAPORE
10 – INSERM (Health&Medical Research) / FRANCE

“Silicon Valley’s hoodie-wearing tech entrepreneurs are the poster kids of innovation. But the innovators who are really changing the world are more likely to wear labcoats and hold government-related jobs in Grenoble, Munich or Tokyo.”
Value Chain for NVM in Leti

Phase-Change Memories

Conductive-Bridge RAM

Customize materials

Innovative design

NVM

Future solutions

TCAD & modeling

Tailored electrical Test

Material Analysis

Critical NVM module development

OXide-Resistive RAM

STT-RAM

A wide toolbox enables customized research with our partners and a benchmark between different BEOL technologies
World "exponentially" larger memory needs

Memory need & technological trend during last decades:

THE PAST:
2002 turnpoint between analog vs digital format

TODAY:
« More Flash chips than grain of rice produced worldwide » (Cappelletti, Micron)

TOMORROW:
No sign of decline or stagnation after ZettaB information in 2012, to when YottaB??

M. Hilbert et al., Vol. 332, SCIENCE, 2011

In billions of GB

0.02
2,62
276,12
18.86

Analog

Digital

Paper, audio tape, photos, vinyl 6.2%
Video tape 9.3%
Other 5.2%
Servers 8.9%
Magnetic tapes 11.8%
DVD/Blu-ray 22.8%
Hard-disk 44.5%
Memory "hierarchy" toward power reduction

- **THE PAST:**
  Strongly hierarchical organization

- **TOMORROW:**
  Lower latency & lower power will be obtained by flattened system architecture, including granular memory possibly non-volatile in BEOL

- **RESULTS:**
  1\ Storage/logic merged → Wire delay reduced, dynamic cons. reduced
  2\ Memory over logic layer → Area reduced
  3\ Non volatile storage → Static power cut off

C. Gopalan, SSE 58 (1) pp. 84-81 (2011)
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RRAM: basic memory operations

Initial state → Low Resistive State (LRS) → High Resistive State (HRS)

FORMING

Low Resistive State (LRS)

RESET

High Resistive State (HRS)

Bipolar switching mode: Write/Erase depend on the voltage polarity
OxRAM technology demonstration

Digital testchip designed by ST with LETI OxRAM active stack:
- \( \text{HfO}_2 \) deposited by ALD
- 10nm Ti deposited by PVD

\[ V_{\text{HV}} \]
\[ V_G \]

Area = 1\( \mu \text{m}^2 \)

ST 65 or 28nm node technology

A. Benoist et al, IRPS 2014, ST/LETI
Variability in the High Resistance State (HRS) reduces the memory operation window: P&V operation appears unavoidable

Variability of the HRS state

No correction code or smart programming algorithms have been used

[M. Azzaz et al., ESSDERC 2015, ST/Leti]
Forming operation in temperature

- Forming process $T^\circ$ activated (0,5V per 100°C)
- Easier forming at HT due to faster defect generation

HfO$_2$/Ti device with initial sub-stoichiometric interfacial layer
Conduction mainly at grain boundaries
Current induced defect generation increases vacancy concentration

T. Cabout et al, IMW 2013
L. Larcher et al, IEDM 2012
SET and RESET operations in temperature

- SET and RESET voltages variation below $\approx 0.05V$ per $100^\circ C$ → stable SET/RESET voltages
Endurance Characteristics

- HRS distribution broader than LRS
- No degradation of the programming window after 108 cycles
Endurance at different temperatures

- Endurance performance does not depend on cycling temperature up to 200°C
Data retention of LRS

- Stability demonstrated on single cells up to 130°C
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Innovative FPGA design thanks to Oxram devices

Ag

GeS₂

HfO₂

W

W/HfO₂/GeS₂/Ag

R_{off} \approx 10^{10} \Omega

Pass Gate + 6T SRAM: 140 F²

Pass Gate + 1T-2R NVE: 20 F²

G. Palma et al., ESSDERC 2013
OxRAM-based Non Volatile Flip-Flop

Flip-Flop core
NV block to store & restore the FF data
Logic block that controls the store and restore operations

- Context saving is performed only before powering down to limit the number of programming operations thus making OxRAM endurance ($10^8$) adequate
NV FF Sleep Energy

Simulations: TiN/HfO$_2$/Ti 28nm CMOS

- Considering 0.5V FF supply in sleep mode, an OXRAM NVFF solution reduces the power consumption with an inactivity longer than 100ms.

N. Jovanovic et al., NEWCAS 2014, Leti
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Memory Advanced Demonstrators (MAD) Technology View

Possibility to explore different integrations for OxRAM, CBRAM, PCRAM and STT-MRAM (with short cycle time)
Cross section of base wafers with CMOS + routing

LETI INTEGRATION

Foundry CMOS

ReRAM demonstrator
Memory Advanced Demonstrators (MAD) Design View

Single Cell 1T1R
- Material/ interfaces assessment
- NVM module analysis
- « Tailored » electrical tests

Small arrays & Crossbar (ex: 8x8)
- Neighbors effect deep investigation
- Direct NVM access
- « Tailored » electrical tests

Large arrays (up to Mb)
- Statistical effect acquisition
- NVM access through decoder
- « tailored » electrical tests after decoding

Complex memory circuits (Auto-test,…)
- Fine tuning statistical analysis
- Electrical tests by digital tester

Versatility (different selectors, voltage/current/time variations…)
Design complexity

Material/ interfaces assessment
NVM module analysis
« Tailored » electrical tests

Statistical effect acquisition
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Fine tuning statistical analysis
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Single Cell 1T1R

Design View

Memory Advanced Demonstrators (MAD)
MAD200 already running & MAD300 for 2017-2018

MAD versions:
• MAD200 → 8” wafers, 130 nm, with techno & PDK for RRAM, PCRAM, MRAM running in LETI cleanroom
• MAD300 → 12” wafers, 28 nm, forecasts first silicon out in 2017
CONCLUSION

MAD200 is a Leti demonstrated success for RRAM and MRAM and PCRAM ...

• MAD approach: versatile test vehicle to make:
  ▪ fast screening of major BEOL NVM technologies (ie RRAM, MRAM, PCRAM)
  ▪ & associated complex design (ie PDK)

• Clear roadmap on 130 nm, 200 mm with 2 further tapeout in 2017

• Tentative roadmap to export the same approach on 300 mm with first silicon out end 2017.

• Leti & CMP offer opening of HfO2-based OxRAM
Thank you for your attention
PTMEM (Memory module) process

Conventional materials memory stack (MxO,...) $\Rightarrow$ RIE Etching

Exotic materials memory stack (MgO,magnetic, Cu...) $\Rightarrow$ IBE Etching
MAD – matrix parametric tester

Example of complete assessment over voltage/current/time & resistance distributions

- A specific setup is available to test memory arrays for MAD mask set
1T1R - 4kbits - 64kbits – 1Mbit comparison

- Same overall behavior in 1T1R, 4kbit and 1Mbit