



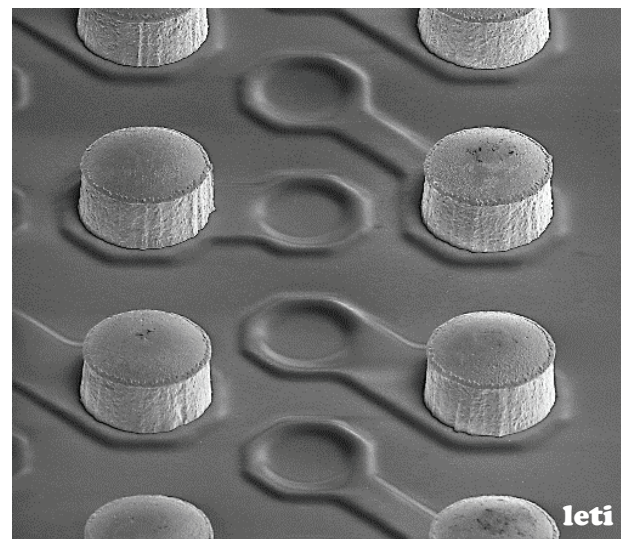
Introduction

Enlarge CMP Packaging Services Portfolio

- Offering advanced, high performances and low cost packaging solutions

Flip-Chip & Advanced packaging advantages

- **Improving IC performances:**
 - Reducing parasitic
 - Increasing I/Os output speed & bandwidth
 - Improving precision
 - Reducing losses
- **Minimizing the assembly footprint**
 - Miniaturization
 - Optimized routing
- **Increasing thermal dissipation**



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-  **Die Level Flip-Chip service**
-  **ams Wafer Level bumping**
-  **Silicon Interposer**
-  **OPEN 3D Post-process**
-  **2017 perspectives**

Wafer-Level Services

Die Level Flip-Chip prototyping:

- **Major constraints**

- Complex process flow
- High engineering effort
- Long processing delays
- Increased cost & failure risk

CMP cost reduction strategy:

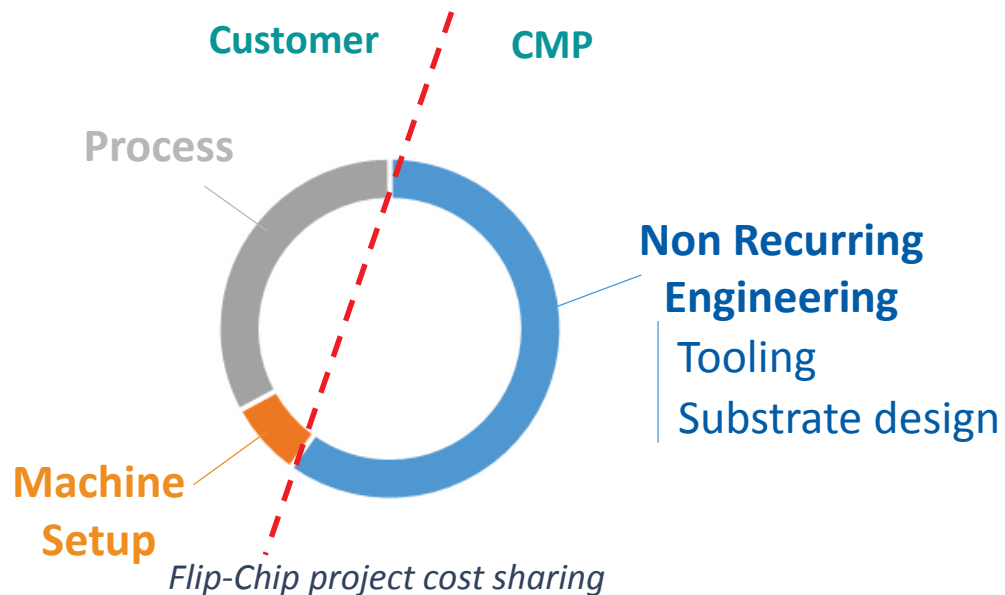
- **CMP takes in charge NRE costs**

- **Using pre-specified packaging properties of the circuit:**

- Die size - I/O pin count - Die thickness - Passivation opening position

- **Turn around time optimization**

- Single procedure avoiding case by case processing
- Prequalified subcontractor engineering effort





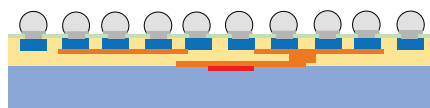
Die level Flip-Chip service

Die Level Flip-Chip on Organic Substrates

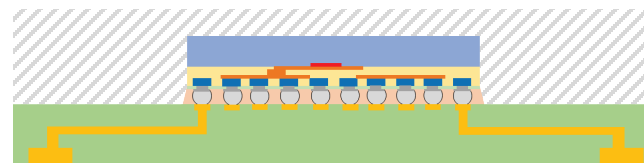
- After standard CMP MPW Runs, single dies undergo a series of steps :
 - Under Bump Metallization deposition
 - Solder balls deposition
 - **Fabrication of plastic LGA package**
 - Flip-Chip assembly on plastic LGA package by mass reflow
 - Underfilling
 - Molding



Standard MPW die



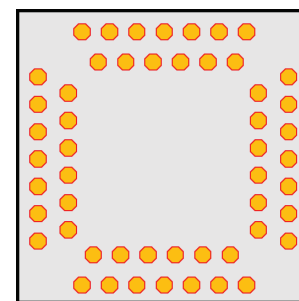
UBM & Solder ball deposition



Flip-Chip on plastic package & Molding

- **Evaluated LGA packages:**
 - 56 I/Os optimized for ST designs
 - 84 I/Os optimized for ams designs

CMP is currently evaluating this process



56 I/Os Pading exemple

Die Level Flip-Chip on Ceramic Substrates

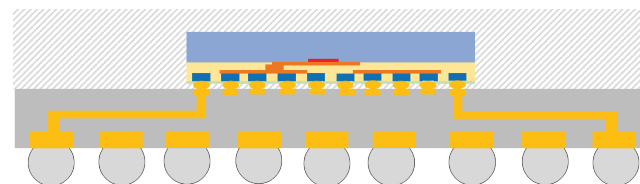
- After standard CMP MPW Runs, single dies undergo a series of steps :
 - Gold Stud bump bonding
 - Fabrication of ceramic BGA package
 - Flip-Chip assembly on BGA ceramic package by thermocompression with NCP
 - Molding
 - Backside BGA balling



Standard MPW die



Gold stud bump bonding



Flip-Chip on ceramic package +
Molding & backside balling



- Evaluated BGA packages:
 - 44 I/Os, 68 I/Os, 84 I/Os, 100 I/Os & 224I/Os

CMP is currently evaluating this process

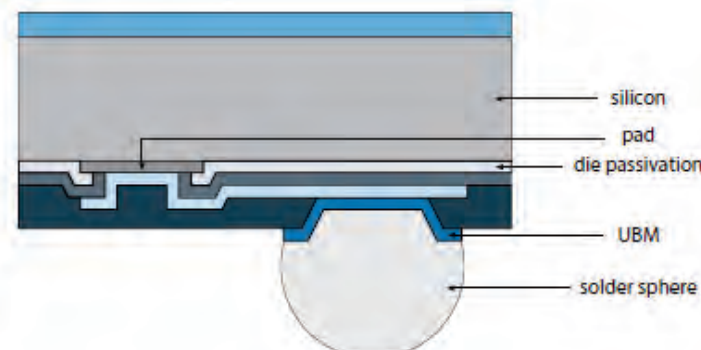


ams Wafer Level bumping



In partnership with ams, CMP offers a bumping service at wafer level on **any 0.35 μ m** and **0.18 μ m** MPW run :

- Forming an evenly **distributed array** over chip surface
- Electrical connections to CMOS pads with **RDL layer**
- **I/O Pitch** compatible with **PCB assembly** processes



Wafer-level bumping option is supported within ams hit kit upon request.
Bumping option is available for a flat fee of 6200 € per design (for 25 chips delivered).



Silicon Interposer

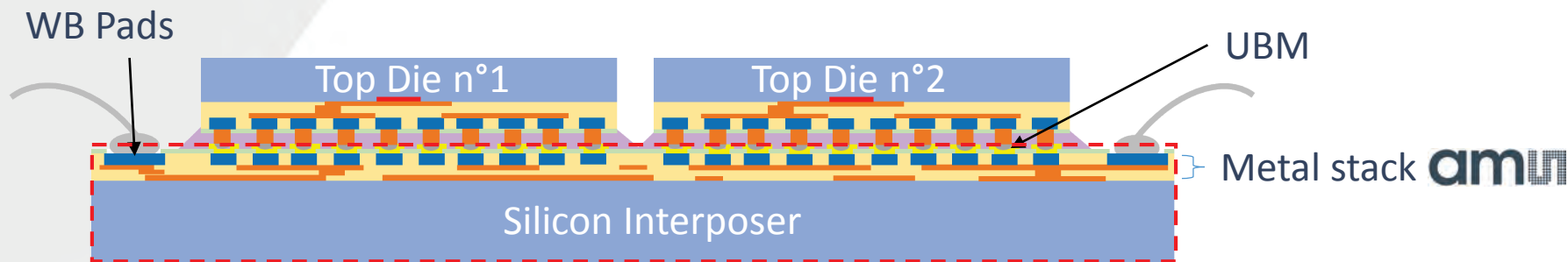
CMP offers a service for two types of **Silicon Interposer** prototyping, in partnership with ams.

Passive Interposer : **Only the backend**, for high density routing and passive components integration.

Active Interposer : **Active layer available** for CMOS integration, allowing a wider range of applications.

Features:

- 4 layer metal stack (Thick last metal) manufactured at ams foundry
- Under Bump Metallization (Ni/Pd/Au) post-processed by sub-contractor
- Interposer includes wire-bond pads to allow its connection to a PCB, or a compatible package



Prices (30 interposers):

Passive interposer 40000 € (< 300 mm²) / Active interposer 50000 € if area < 100 mm²

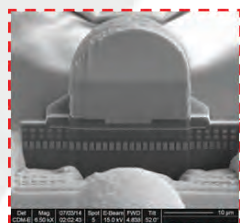
64000 € if 100 mm² < area < 200 mm²

OPEN 3D post-process allows 3D interconnection integration on various technology nodes. Modules are integrated at wafer level after standard MPW.

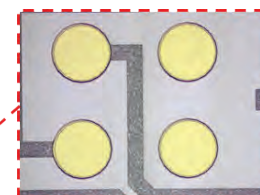


Front-side modules:

- μ -Bumps
- UBM



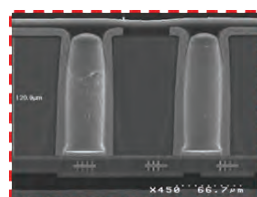
μ -Bumps



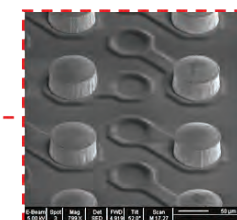
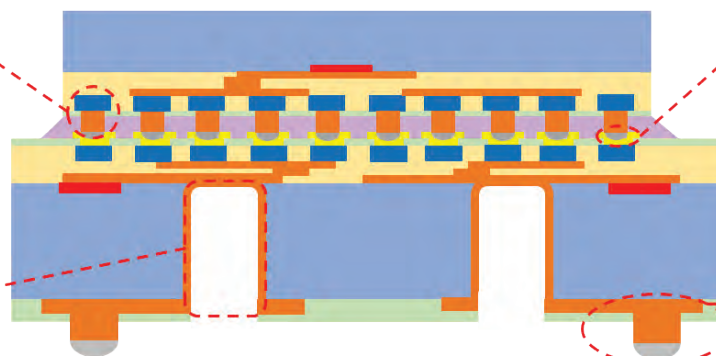
UBM

Back-side modules:

- TSV last
- RDL
- Bumps



TSV-last

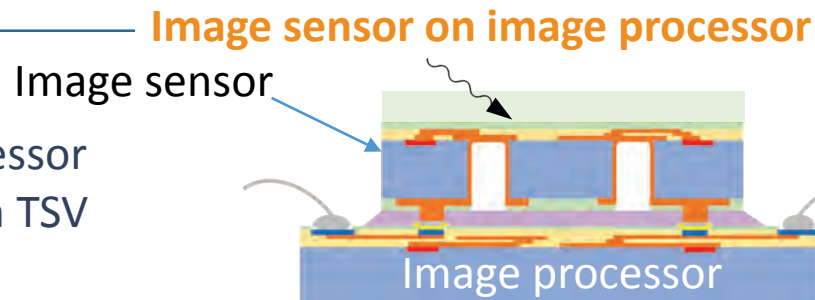


RDL + Bumps

Bumps	Cu/SnAg ; \varnothing 65 μ m ; 120 μ m min pitch ; ~ 60-70 μ m thickness
Micro-bumps	Cu/SnAg ; \varnothing 25 μ m ; 50 μ m min pitch ; ~ 20 μ m thickness
UBM	TiNiAu ; 30 μ m width min ; 50 μ m min pitch ; 1 μ m thickness
TSV-Last	\varnothing 60 μ m x 120 μ m depth ; 120 min pitch
Backside RDL	Cu ; 20 μ m min width ; 40 μ m min pitch ; 4-8 μ m thickness

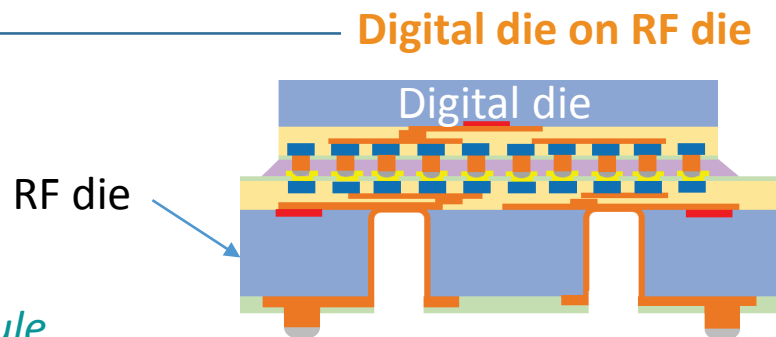
- Small footprint
- 2 heterogeneous nodes for sensor and processor
- Top-die frontside access to light sensing with TSV

Application : Image sensor in embedded devices



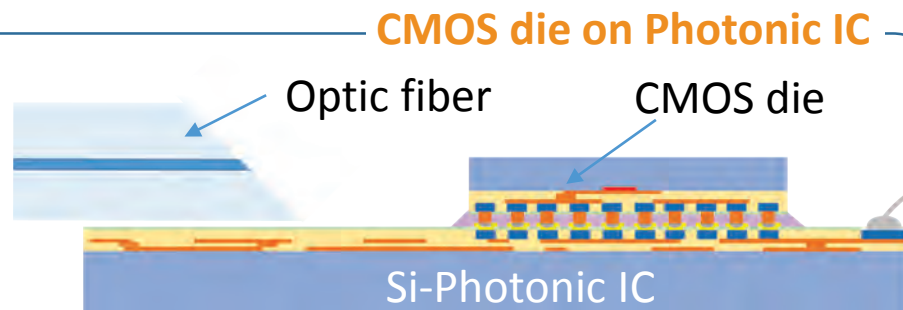
- High bandwidth between dies
- 2 heterogeneous nodes for :
 - High density digital die
 - Radio-frequency die

Application : Processor on RF communication module



- Electronic die integration on Photonic IC

Application : Data center, HPC



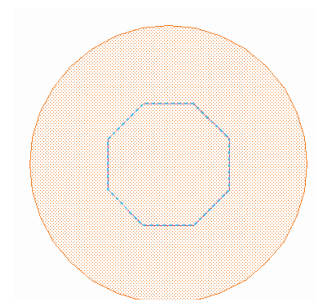


OPEN 3D Design & verification tools

Post-Processed die combines two technologies, thus requiring a special consideration during design, verification and fabrication

3D Design kit

- As an add-on to the foundry kit
- OPEN 3D post-process technology **integration to cadence**
- Specific **additional libraries** (Bumps, μ -bumps, TSV...)
- Specific calibre **die-level DRC** deck
- Specific **documentation** (DRM, tutorial ...)



μ -bumps layout

Assembly-level verifications

- Run with calibre 3DSTACK
- Die-to-die **layout verification**
- Die-to-die **electrical connection verification**

} Require a project-specific development

Designing a 3D post-processed die can be confusing for someone used to classical 2D projects. CMP will take a special consideration to guide designers every step of the way for achieving their 3D projects.



OPEN 3D Prices & schedule

Post-Process options and prices

Front-side: μ -Bumps or UBM

For ams 0.35 μ m and ST 130, 65, 55 and 28nm CMP MPW

22500 € + additional fees *

Back-side: TSV, RDL and Bumps

For ams 0.35 μ m ST 130nm, 65nm and 55nm CMP MPW

53500€ + additional fees *

- OPEN 3D post-process MPW runs are subject to a sufficient level of participation
- *Additional fees are applied function of the silicon MPW technology: 6.5k€ in 0.35 μ m ams/ 3.4k€ in 130nm STM/ 9k€ in 65nm STM/ 11k€ in 55nm STM / 13.5k€ in 28nm STM.
- Dedicated runs are made available at any time, please contact CMP

Schedule

Open 3D-CMP post processes are available on the last MPW runs of the year for the following technologies:

	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
IC 28nm CMOS28FDSOI	30			15					← TBD →			
IC 55nm BiCMOS055			21			8				27		
IC 65nm CMOS065			9			22				19		
IC 130nm BiCMOS9MW		23					12				22	
IC 0.18 μ m BCD8SP			10						11			
IC 0.35 μ m RF C35B4M3		27				6			11			11
Photonic MPW Prototyping Si310-PHMP2M			6						11			

* Schedule on January 2017 – Run dates are subject to changes



Die-level Flip-Chip services

- **Evaluating the proposed options:**
 - CMP made an investment to evaluate the feasibility
 - Test ICs and substrates have been designed and manufactured
 - Assembly & characterization of prototypes are in progress
- **Making the offer available during 2017**
- **Working on a stud bumping offer at die level as stand alone**

Wafer-level services

- **Widening our wafer-level bumping offers**



Thank you !

