3D TECHNOLOGIES WAFER SERVICES AT LETI FOR CMP MULTI-PROJECT-WAFER

LETI CONFIDENTIAL

CMP annual meeting| Parès Gabriel

Top chip : 45 nm
Bottom chip (130nm)
Interco
TSV
Board
Introduction: 3D at Leti

Leti 3D stacks proposed in CMP MPW offer - illustrations

3D technology modules
• Process
• Illustrations
• Design Rules

Work flow
ABOUT CEA-LETI

French R&D institute in microelectronics & nanotechnologies from

- 1,700 researchers
- Over 2,200 patents
- 250 M€ annual budget
- 50 start-ups
- & 365 industrial partners

- ~100 people working on 3D IC and 3D Packaging
- Full 200mm & 300mm 3D capabilities
LETI organization and Lab overview

**LETI**

- **DCOS** [silicon component]
- **DTSI** [Si platform]
- **DOPT** [optical sensors]
- **DACLE** [IC design]
- **DTBS** [Biology-health]

- **SCME** [CMOS] [3DIC]
- **SCMS** [sensors] [MEMS] [µ-systems] [interposers] [3D packaging - Integration]
- **SCPE** [Power] [Energy]

Lab for packaging / interposer / 3D integration

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**Objectif:** Valider une plateforme générique d’intégration 3D (conception, technologies et caractérisation), permettant le prototypage d’applications.

**Moyens :**
- Développer les technologies génériques pour l’intégration haute densité
- Développement des outils de conception et de méthodologies de tests à l’échelle de la plaque et du système packagé
- Validation sur des démonstrateurs technologiques
To solve the following issues:

- **Form factor decrease:**
  - X & Y axis
  - Z axis

- **Performances improvement**
  - Decrease R, C, signal delay
  - Increase device bandwidth
  - Decrease power consumption

- **Heterogeneous integration**
  - Integration of heterogeneous components in the same system

- **Cost decrease**
  - Si surface decrease
  - Reuse of existing Packaging, BEOL & FEOL lines
3D/2.5D: A “GENERIC” SOLUTION?

HD interposers ➔ Coarse interposers

**High performance computing**
High-end servers

- 3D stack on interposer
- ~150 - 200W

**FPGA**

- XILINX
- Next Generation integration (Si-interposer / TSV)
- SIP (Through silicon via)
- High-end servers

**Mobile**

- PoP still there!!
- Supply chain
- 5-10 Watts
- 12 - 50 Gbps

**3D Imaging**

- 3D technology for tracker
- <40µm pixels
- Read out circuit at the back
- Ultra fine routing at the interposer backside

**Passive /active**

- HD interposers
- Coarse interposers

From Fujitsu

Ultra fine routing at the interposer backside
Particles detectors: Mmw platform:
4G with TSV:
X-rays/particles dead zone free detectors

Medical applications
High perf. Passives (Capa→1µf/mm²)

radar, military, space

Consumers
Power amplifier (PA) 4G with TSV:

Fondamental physics

3x3 mm²
130nm SOI CMOS 60µm TSV

Medical applications
75µm TSV
40% size decrease vs. organic

TSV-LAST COARSE INTERPOSERS DEVELOPMENTS AT LETI (2010 -2014)
### 3D ‘GENERIC’ TECHNOLOGY TOOLBOX

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<td>Temp. Bonding (slide off)</td>
<td>High throughput P&amp;P</td>
<td>Thick Polymer molding</td>
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<td>Solder balls</td>
<td>TSV Middle &amp; BS AR10</td>
<td>Temp Bonding (Zonebond)</td>
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<td>Thin Polymer molding</td>
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<td>μinserts</td>
<td>Copper pillar</td>
<td>TSV Last AR1</td>
<td>Temp. bonding (Peeling)</td>
<td>Self Assembly</td>
<td>Thin Oxide planarization</td>
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<td>μtubes</td>
<td>DTW Cu-Cu</td>
<td>TSV Last AR2</td>
<td>Permanent bonding</td>
<td>Wafer To Wafer</td>
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<td>Cu-Cu</td>
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<td>TSV Last AR3</td>
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<td>Permanent bonding</td>
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<td>TSV Last High density</td>
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</table>

**Handling:**
- Temp. Bonding (slide off)
- Temp Bonding (Zonebond)
- Temp. bonding (Peeling)
- Self Assembly
- Permanent bonding
- Wafer To Wafer

**Die Placement:**
- High throughput P&P
- High precision P&P
- Self Assembly
- Permanent bonding
- Wafer To Wafer

**WL Molding:**
- Thick Polymer molding
- Thin Polymer molding
- Thin Oxide planarization
- WLUF
- Classic Underfill
Technological modules implemented by OPEN3D™:

- Through Silicon via (TSV)
- Redistribution layer (RDL)
- Under Bump Metallization (UBM)
- 3D Interconnections
- Components stacking
- Packaging with partner collaboration

Wafers (bottom and/or top dies) provided by costumer
CMP MPW 3D OPTIONS

Die-to-die

Flip chip stacking +WB

Die-to-substrate

Die-to-passive interposer

Wire bonding

μbumps

Passive Si interposer

FS RDL/Bumps

BGA substrate

Top die

Bottom die

Top die

Top die

Top die

Flip chip stacking + TSV last/RDL

TSV last/RDL

Active die

μbumps

TSV/BS RDL/Bumps

Passive Si interposer

Active interposer
3D INTERCO FOR FLIP-CHIP ASSEMBLY

3D technological modules fabrication at wafer level with MPW design
- Top die: µ-bumps
- Bottom die: UBM or copper pillars

Components stacking
- Die-to-die
- Die-to-wafer
- Die-to-passive interposer
- Die-to-BGA substrate

Technology nodes offer:
- 200 mm: CMOS130, BICMOS9, AMS techno
- 300 mm: CMOS65/FDSOI28 (all options)

Flip chip by pick&place and solder reflow (collective or thermo-compression): Leti or outsourced

Example
- Top die with µbumps
- Wire bonding
- Bottom die or interposer
- CMOS130
- Flip-chip assembly
Micro-bumps DRM & schematic

- Wafer size: 200 mm
- Micro-bumps material: Cu post / SnAg 305 solder
- Minimum pitch: 50 µm
- Minimum micro-bumps diameter: 25 µm
- Micro-bumps thickness (typical): Cu 10µm / SnAg 10µm

Micro-bumps Morphological illustrations

Micro-bumps before reflow

Micro-bumps after reflow

Micro-bumps on C65
D = 25 µm

Micro-bumps on FDSOI28
D = 18 µm
Wafer size: 200 mm
Landing micro-bumps material: Cu post / NiAu protection possible
Minimum pitch: 50 μm
Minimum landing micro-bumps diameter: 25 μm
Typical landing micro-bumps thickness: Cu 10μm / NiAu 1.2μm

Landing micro-pills with protective layer
Landing micro-bumps w/o protective layer
Landing micro-pillar on top metal

Au capping
Ni diffusion barrier
Cu base
**UBM DRM & schematic**

- **Wafer size:** 200 mm
- **UBM material:** TiNiAu
- **UBM thickness:** 1 µm
- **UBM minimum width:** 25 µm
- **UBM minimum pitch:** 50 µm

**UBM Morphological illustration**

Backside and frontside UBM possible

On top of Alu or Copper Pad

Different shape possible:
- Square
- Polygons
- Circle

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OPEN 3D™ TECHNOLOGICAL OFFER

UBM

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**OPEN 3D™ TECHNOLOGICAL OFFER**

**SOLDER BUMPS**

**Bumps DRM & schematic**

- Wafer size: 200 mm
- Pillars material: Cu stud / SnAg solder
- Minimum pitch: 120 µm
- Pillars diameter: 65 µm
- Pillars thickness: Cu 35-40 µm / SnAg 25-30 µm

**Pillars Morphological & electrical results**

**Bumps characteristics**

<table>
<thead>
<tr>
<th>Bumps</th>
<th>R (mΩ)</th>
<th>Elec. Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bumps</td>
<td>50</td>
<td>100 %</td>
</tr>
</tbody>
</table>

**Solder bump**

**Metal 1**

**TSV**

**RDL**

**Passivation**

**Cu stud**

**Solder alloy**

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Technological modules fabrication at wafer level with MPW design

- Front side: Alu pad finish (WB) or μ-pillars (Cu/TiAu) or UBM (TiNiAu) for Flip-chip assembly
- Wafer thinning on temporary carrier at 120µm
- Back side: TSV, RDL, UBM or solder bumps

Components stacking

- Die-to-die
- Die-to-wafer

Technology nodes offer:

- 200 mm CMOS130 /BiCMOS9
- 300 mm CMOS65

Flip chip by pick&place and solder reflow (collective or thermo-compression)
TSV DRM & schematic

- Wafer size: 200 mm
- Wafer thickness: 120 µm
- TSV type: via last / Cu liner
- Minimum pitch: 120 µm (for 60µm TSV)
- TSV diameter: 60 µm
- Aspect Ratio (AR): from 1:2

TSV morphological & electrical results

TSV-last AR 2:1

Electrical tests results

TSV characteristics

<table>
<thead>
<tr>
<th>TSV geometry</th>
<th>R (mΩ)</th>
<th>C (pF)</th>
<th>Elec. Yield</th>
<th>Insul. (MΩ)</th>
<th>I_{leak} (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV_{60/120}</td>
<td>19.1</td>
<td>0.82</td>
<td>100 %</td>
<td>&gt; 100</td>
<td>1.3 10^{-9} @ 10V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.1 10^{-9} @ 50V</td>
</tr>
</tbody>
</table>
Metalization: requires to use low temperature processes (< 250°C / < 200 °C)

Barrier / seed layer deposition: PVD/CVD Ti/Cu deposition

Electroplating
- Cu liner or Cu filling
- Choice of electrolyte: 2 or 3 additives
- DC or pulse current
- Hydrodynamic conditions

Source: K. Crofton / Aviza / Semicon 2009
Source: Dow
Source: CEA-LETI
**TSV-LAST EXAMPLE**

TSV top:
- Oxide liner = 1.5-1.8 µm
- Cu liner = 7.5 µm
- Passivation cap = 14 µm

TSV bottom corner
- Oxide liner = 0.43 µm
- Cu liner = 3.7 µm

TSV bottom
- Cu liner = 3 µm
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BACK SIDE RDL

**RDL DRM & schematic**
- Wafer size: 200 mm
- RDL material: Cu
- RDL thickness: 4-8 µm
- RDL minimum width: 20 µm
- RDL minimum space: 20 µm
- Passivation layer: Polymer (several materials available) or mineral

**RDL Morphological & electrical results**

Backside Cu RDL

<table>
<thead>
<tr>
<th>RDL characteristics</th>
<th>Insolation between lines</th>
<th>$I_{\text{leak}}$ @ 10V (A)</th>
<th>Elec. Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDL</td>
<td>&gt; 6.0 GΩ</td>
<td>$1.6 \times 10^{-9}$</td>
<td>100%</td>
</tr>
</tbody>
</table>

Cu RDL integration: Solder bumps on RDL + passivation
EXAMPLE 1 = ACTIVE SI INTERPOSER WITH PARTITIONING

- Analog & digital partitioning: 45 nm on 130 nm
- Technology node splitting: Advanced for digital / Mature for Analog
- + Cost: no need to use advanced techno for mature components

Source: CEA-LETI / ST Micro
**EXAMPLE 2 = PIXEL SENSOR**

**TSV Medipix3/RX results – 2012-2014**

- **Back side UBM**
- **Accoustic image of the bonding interface**
- **Thin wafer debonded on tape**
- **RDL Cu 7 µm**
- **TSV 60µm x120µm**

**Technology**

- **Medipix wafer after front side UBM**

**Electrical Tests**

- **2 TSV chain resistance**

**Contact UBM**

**Functional tests on ASICs**

5 lots run at LETI
Die to die, Die to wafer, Die to substrate, multi dies heterogeneous stacking

- Die size: 0.5x0.5 to 15x15 mm
- Die thickness: 50 to 725 µm
- Wafer size: 200 & 300 mm
- Wafer thickness: 100 to 725 µm
- Solder bumps interconnect: Cu stud / SnAg 305 solder on UBM (TiNiAu) or Cu/TiAu
- Minimum pitch: 40 µm
- Solder pillar diameter: 20-80 µm
- Stand off: 10-60 µm
- Underfilling: Capillary

Chip stacking illustration
DIE-TO-WAFTER STACKING WITH MBUMPS/UBM

Wafer yield = 94%

Yield vs Nb of μbumps

Daisy chain Resistance (Ω) = f(nb of μbumps)

\[ y = 0.1657x \]

\[ R^2 = 0.9977 \]
3D WORK FLOW WITH CMP

 CMP MPW wafer service
- 3D modules identification
- order form

LETI
3D Technology implementation
- Interconnections
- TSV
- Metalization
- Components stacking

Wafer fabrication in foundry
Wafer reception at LETI

Design & Layout & DRC

Dicing & Packaging

3D Electrical Tests

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Merci de votre attention