Open 3D™ Platform

Annual review CMP - 2013

D. Henry / A. Berthelot / R. Cuchet

CEA-Leti-Minatec

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Outline

- Introduction / Concept
- Technological offer
- First success stories
- LETI-Open 3D & CMP collaboration
Introduction: What is 3D Integration?

- In electronics, a 3D integrated circuit is a chip in which two or more layers of active electronic components are integrated vertically into a single circuit, component or system.

3D Integration key drivers:
- Form factor decrease
- Performances improvement
- Heterogeneous integration
- Cost decrease
The concept:

- Objective: to fill the gap between R&D & products industrialization
- Open 3D™ is a 3D technology offer, targeting industrial & academic customers
- Open 3D™ will give access to 3D innovative technologies with the following key drivers:
  - Light R&D investment: Based on existing technologies
  - Customization upon request
  - Short cycle time
    - 200 mm & 300 mm (2013)
- Global offer from 3D design to component final packaging
- Possibility to make proof-of-concept, prototyping & small volume production

Open 3D customer’s typology:

- Laboratories, universities and international Institutions
- Fabless
- “Niche” markets manufacturers & integrators
- IDM
Technological offer overview

Open 3D™ TechBox
As a Lego™ approach

Design & Layout
- DRM
- Masks
- DK 3D

3D Technology
- TSV

Electrical Tests Yields
- Parametric
- Process
- SPC

Reliability (Q2 2013)
- TCT
- HAST
- EM

Interconnections

Metalization

Components stacking

Packaging
Technological offer overview – 3D technologies zoom

- Technological modules definitions:
  - Through Silicon via (TSV)
  - Redistribution layer (RDL)
  - UBM
  - Interconnections
  - Components stacking
  - Packaging with partner collaboration

![Diagram of 3D technology components]

- Top die
- Front side UBM
- Bottom die or interposer
- RDL
- Back side UBM
- Micro-bumps
- Micro pillars
- TSV
- Passivation
- Bumps
- Pillars
- Substrate or BGA or package
First success story: Open 3D™ for CERN

**CERN Project summary**
- Product: XRay detector for medical applications
- Project started: On June 2011
- First wafers delivered: on January 2012
- On schedule / Results OK

**CERN Project Results**
- Design
- Test structures
- Wafer view
- Single chip

**Process Flow**
First success story: Open 3D™ for CERN

CERN Project Results

Technology

- Back side UBM
- Medipix wafer after front side UBM
- Accoustic image of the bonding interface
- Thin wafer on tape
- RDL
- TSV

Electrical Tests

- Contact UBM
- TSV
- 2 TSV chain resistance

Preliminary results using a 3D integration technology for hybrid pixel detectors designed for particle physics and imaging experiments
A. Berthelot(1), D. Henry(1), R. Cuchet(1), C. Chantre(1), M. Campbell(2), T. Tick(2, 3) / MINAPAD 2012

Functionnal tests on ASICS

3D Integration Technology for Hybrid Pixel Detectors Designed for Particle Physics and Imaging Experiments
D. Henry(1), A. Berthelot(1), R. Cuchet(1), C. Chantre(1), M. Campbell(2), T. Tick(2, 3) / ESTC 2012
Open 3D™ Second project : Cassidian

- Product: RF component for telecom
- Including TSV + backside bumps
- Project started On June 2011
- First wafer delivered in February 2012
- Final Electrical results OK

Cassidian Project Results

Design
- Single chip

Techno
- Front side view
- Back side TSV + RDL
- Back side TSV + RDL + bumps

Electrical Tests
- 2 TSV chain resistance
Open 3D™ / CMP collaboration

- Simple and moderate cost process for customer

Specific conditions to access wafers from CMP:
- One extra mask to hide other customers contributions
- Other customers chips return to CMP after 3D process (wafers skeletons)
Open 3D™ / CMP collaboration – First project

- Application: RF Power Amplifier (PA)
  - Multiband & Multi-standard for cellular 4G
  - Ground connection is critical for high performance RF power applications
  - TSV benefits
    - Reduced ground inductance => Improved power gain
    - Improved thermal dissipation
    - Allows reduced die area
    - Provides design flexibility
    - Simplified ground connection for on-chip components

- CMP Technology targeted: ST SOI 130nm (HCMOS9-SOI)
- Wafers from CMP to Open 3D
- TSV last 60 µm / Aspect ratio 2:1
- Backside Cu RDL + Au protection

Power gain comparison between TSV, Flip-chip and Wire bonding
(Courtesy of A. Giry / CEA-LETI-DACLE)
Thank you for your attention