BCD Technology

Sense & Power and Automotive Technology R&D

January 2017

Content

- BCD in ST
- Technology platform details

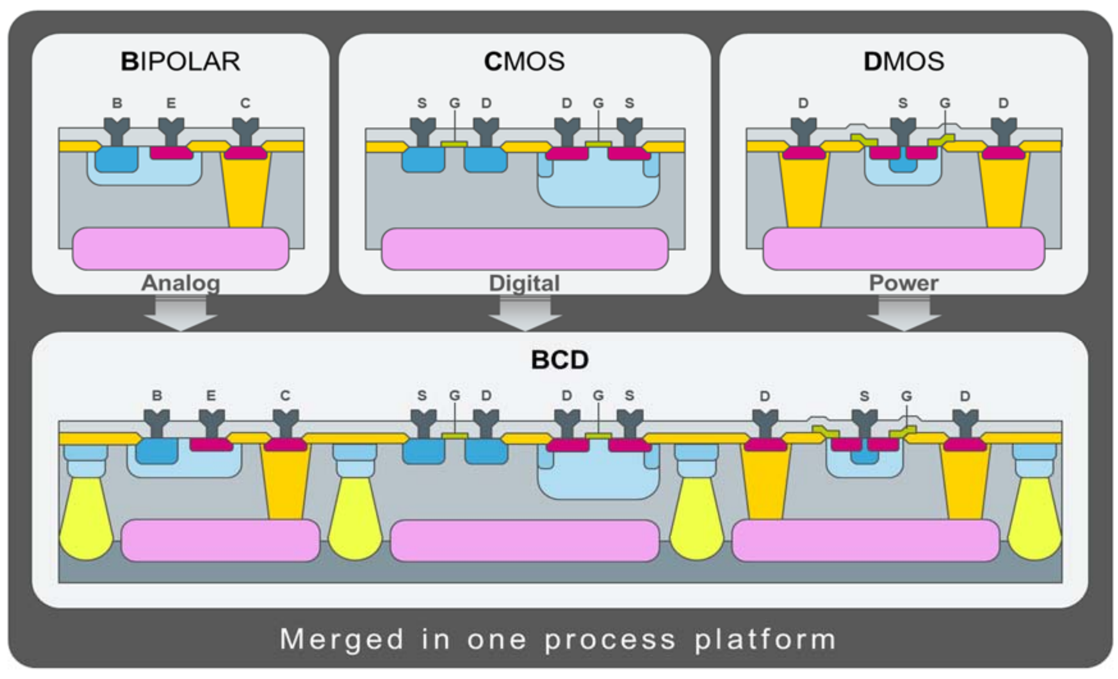
Content

BCD in ST

Technology platform details

What is BCD ?

A concept invented by ST in the mid-80s [1][2][3] widely used today in the industry

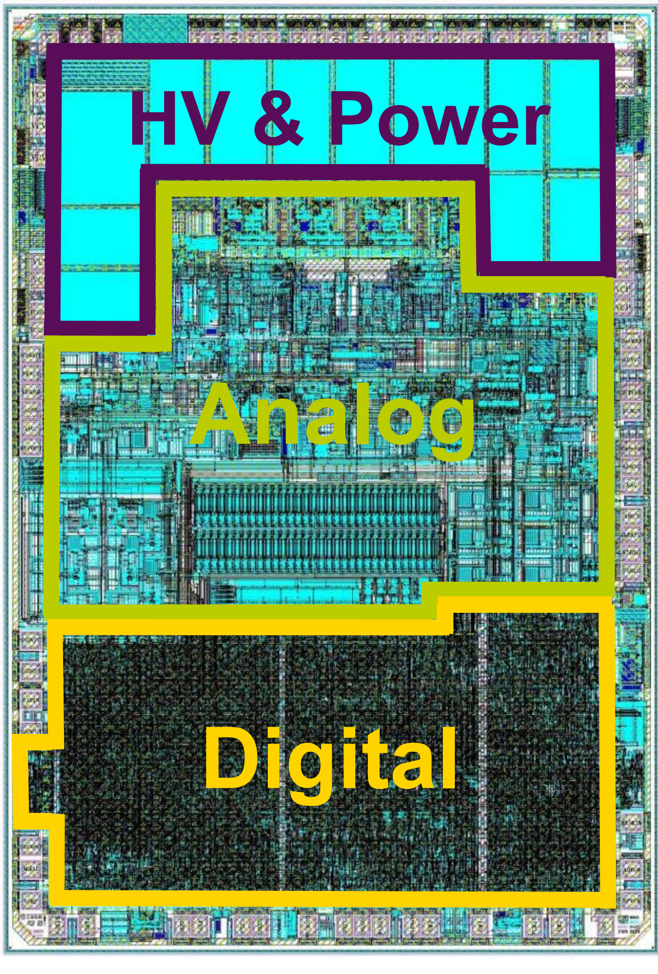


[1] ***Single Chip Carries Three technologies***, Electronics Week, December 10, **1984**

*[2] C. Cini, C. Contiero, C. Diazzi, P. Galbiati, D. Rossi, "**A New Bipolar, CMOS, DMOS Mixed Technology for Intelligent Power Applications"***, ESSDERC '85 Proceedings, Aachen (Germany), September **1985**

*[3] A. Andreini, C. Contiero, P. Galbiati, "**A New Integrated Silicon Gate Technology Combining Bipolar Linear, CMOS Logic and DMOS Power Parts**"*, IEEE Transactions on Electron Devices, Vol. ED-33 No.12, December **1986**

Analog + Digital + Power & HV on one chip



High Voltage or Power section (DMOS) to drive external loads

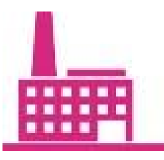
Analog blocks
to interface the “external world”
to the digital systems

Digital core (CMOS)
for signal processing

BCD Roadmap Driving Factors

BCD Evolution in the “More than Moore” arena

Driven more by Process Customization
for Application Requirements
than by Reduction of Lithography Node



Trend towards Advanced Technology Nodes
compatible with availability of
Depreciated Advanced Manufacturing Plants

Long Lifetime
of Products and Process Generations

Always present demand for Cost Reduction

BCD in ST – Overview

- Solid know-how developed over three decades
  - Processes from 4.0 µm to 0.11 µm developed and produced
- Unique voltage range offering
  - Large voltage range spanning multiple application fields
- Advanced process nodes differentiated by application
  - Offers best in class HV devices with large CMOS integration capability
- Process customization by application
  - Strong synergy between technology, design and application

30 Years

5 V to 800 V

0.16 µm
0.11µm

BCD Technology Segmentation

SEGMENT		TECHNOLOGY PLATFORM	APPLICATION FIELDS
High Voltage BCD	0.32µm	**BCD6s Offline** *3.3V / 5V CMOS – 25V/800V/1200V*	Lighting, Motors, Electrical Car
		BCD6s HV Transformer *3.3V CMOS - Galvanic Isolation 4-6KV*	
SOI BCD		**SOI-BCD6s** *3.3V CMOS - 20V/50V/100V/190V*	Full digital amplifier, Echography, AMOLED, Pico-projector
	0.16µm	**SOI-BCD8s** *1.8V CMOS - 70V/100V/140V/200V*	
Advanced BCD		**BCD8sP - 0.16µm** *1.8V CMOS - 10V/18V/27V/42V/60V*	HDD, Airbag, Audio amplifier, Printers, ESP, ABS, Power Line modems, Power Supply, Automotive, Power Management for Mobile
		BCD8sAUTO - 0.16µm *3.3V CMOS - 20V/40V/65V/100V*	
	0.11µm	**BCD9s - 0.11µm** *1.8V CMOS - 10V/40V/60V*	
		BCD9sL - 0.11µm *3.3V CMOS - 20V/40V/65V/100V*	
		BCD9sE - 0.11µm – *e-PCM* *1.8V CMOS - 10V/40V/60V*	
	90nm	**BCD10 - 90nm** *8V to 65V*	

Content

- BCD in ST
- Technology platform details

SOI-BCD8s Overview

SOI-BCD8s is a **0.16µm** Technology Platform dedicated to **High Voltage** applications on **SOI** substrates with the following main features:

- Baseline 3.3V CMOS
- **Medium Voltage Module** including 6V / 20V / 40V N-ch and P-ch MOS
- **High Voltage Module** including 70V/100V/140V/200V N-ch and P-ch MOS
- Optional 2nd gate oxide for 1.8V CMOS
- **Dielectric Isolation on SOI**
- 4 Metal Levels with last AlCu Thick Power metal
- Available memory: OTP

Application examples:

- 3D MEMS scanning, Pico-projector (MEMS µ-mirror driver)
- Consumer and Automotive Audio Amplifier
- Automotive Sensor Interface ICs
- 3D Ultrasound (echography)

SOIBCD8s device portfolio

Device Portfolio

Low Voltage
- 1.8V CMOS (3.5mn oxide)
- 3.3V CMOS (7nm oxide)

Medium Voltage
- N-DRIFT on GOX=7nm
  6V, 20V, 40V
- P-DRIFT on GOX=7nm
  6V, 40V

High Voltage
- N-DRIFT on GOX=7nm
  70V, 100V, 140V, 200V
- P-DRIFT on GOX=7nm
  70V, 100V, 140V, 200V

Bipolar
- 5V NPN
- 5V NPN w/ CPCIMP
- 3.3V PNP

Diodes
- 5V Zener
- p+/Nwell, p+/Nwell3V3
- n+/Pwell, n+/Pwell3V3
- HV Fast Diodes 100V/200V

Capacitors
- 1.8V/3.3V poly P+ on pwell
- 1.8V/3.3V poly N+ on cpcimp (pwell)
- 5V poly-poly HL
- 100/200V MOM
- 30V MOM interdigitated

Resistors
- Poly resistors, including HIPO resistor (1kOhm and 6kOhm/sq)
- Diffused resistors
- Thin film resistor

Trimming
- OTP Antifuse on 7nm GOX

life.augmented

SOI-BCD Highlights

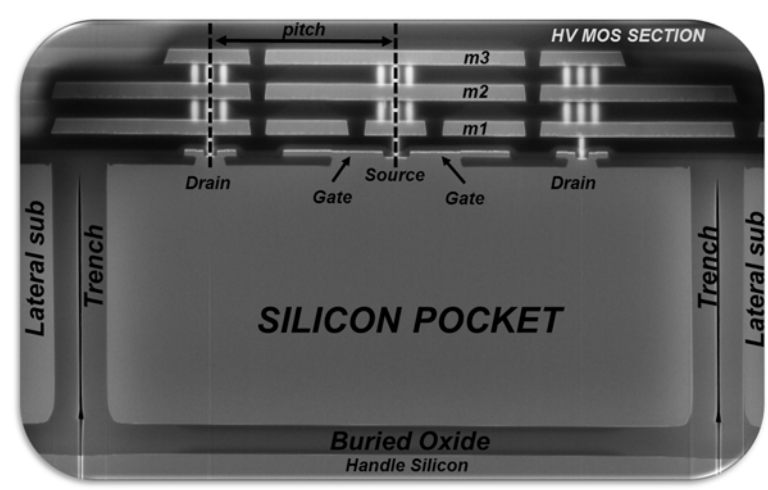
SOI Isolation versus Junction Isolation

Advantages

- Parasitic bipolars elimination
- Reduced isolation distance
- Below Ground capability
- EMI robustness

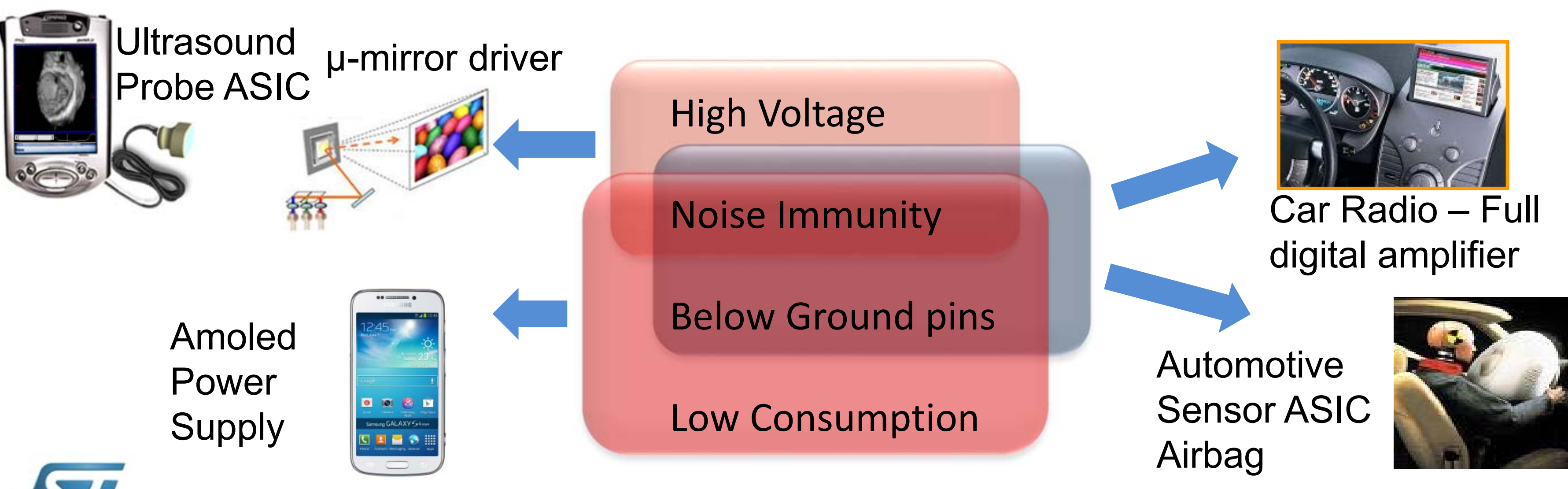
Drawbacks

- High cost of substrate
- Parasitic capacitance
- Thermal effect



Fully isolated HV MOS section

*SOI BCD is **convenient** or even **mandatory** in case of:*



life.augmented

3.3V CMOS

- Nominal operating voltage = 3.3V
- Maximum operating voltage = 3.6V
- Absolute maximum rating = 4.6V
- Nominal Gate-to-Source voltage = 3.3V
- Maximum Gate-to-Source voltage = 3.6V
- Transistor density (4 metal levels) =50000gate/mm^2

Device	Gate length [µm]	Vth (mV) (physical) @Vds=0.1V Intercept with Vgs axis at Gm peak			Vth (T.C.) (mV/°C)	Ioff/W_{sh} pA/µm @Vds=3.3V @ T=150°C	Idsat/W_{sh} µA/µm @Vgs=3.3V
		Min	Typ	Max			
3.3V NMOS W=10µm	0.35	809	892	970	-1.12	9.93	374.3
	10	695	753	811	-1.12	4.25	36.35
3.3V PMOS W=10µm	0.35	-845	-940	-1029	-1.16	6.64	202.6
	10	-851	-918	-986	-1.12	5.61	7.29

Device	MATCHING	
	$\sigma(\Delta Vth) = a_0 * (W_{sh}*L_{sh})^{-0.5}$	$\sigma(\Delta\beta/\beta) = b_0 * (W_{sh}*L_{sh})^{-0.5}$
3.3V NMOS	a_0= 7.4mV*µm	b_0= 2.01%*µm
3.3V PMOS	a_0= 5.47 mV*µm	b_0= 1.27%*µm

1.8V CMOS

- Nominal operating voltage = 1.8V
- Maximum operating voltage = 2.0V
- Absolute maximum rating = 2.5V
- Nominal Gate-to-Source voltage = 1.8V
- Maximum Gate-to-Source voltage = 2.0V
- Transistor density (4 metal levels) =90000gate/mm^2

Device	Gate length [µm]	Vth (mV) (physical) @Vds=0.1V Intercept with Vgs axis at Gm peak			Vth (T.C.) (mV/ºC)	Ioff/W_{sh} pA/µm @Vds=1.8V @ T=150ºC	Idsat/W_{sh} µA/µm @Vgs=1.8V
		Min	Typ	Max			
1.8V NMOS W=10um	0.18	508	597	671	-0.76	1503	665
	10	368	433	498	-0.78	146	24.24
1.8V PMOS W=10um	0.18	-464	-556	-633	-0.91	1267	259
	10	-485	-549	-614	-0.85	10.6	3.69

Device	MATCHING	
	$\sigma(\Delta Vth) = a_0 * (W_{sh}*L_{sh})^{-0.5}$	$\sigma(\Delta\beta/\beta) = b_0 * (W_{sh}*L_{sh})^{-0.5}$
1.8V NMOS	a_0= 4.79mV*µm	b_0= 1.1%*µm
1.8V PMOS	a_0= 3.44 mV*µm	b_0= 0.86%*µm

HV MOS and Bipolar electrical parameters

	Maximum operating voltage [V]	6	20	40	70	100	140	200
N-CH	R_{ON}xArea [mΩ·mm^2] (typical) @ V_{GS}=3.3V	2.15	26	33	115	245	390	900

	Maximum operating voltage [V]	6	40	70	100	140	200
P-CH	R_{ON}xArea [mΩ·mm^2] (typical) @ V_{GS}=-3.3V	11.7	113	375	740	1440	3570

Device	Gain typical	BV_{CEO} [V] typical	V Early [V]
NPN 5V	6	18.5	165
NPN 5V Cpc-impl	120	18.5	100
PNP 3.3V	55	-13.0	7.5

Resistors electrical parameters

Resistor type	Rsheet [Ω/sq]	Non Linearity factor (W=5µm)	Temperature coefficient	Mismatch σ(ΔR/R) [%·µm]
Nwell	666	0.18%/V	TC1=4.15e-3 $°C^{-1}$ TC2=9.97e-6 $°C^{-2}$	0.93
Nminus	2930	5.9%/V	TC1=-0.94e-3 $°C^{-1}$ TC2=12.4e-6 $°C^{-2}$	0.54
Unsilic. P+ poly	330	-48e-6/V	TC1=-0.14e-3 $°C^{-1}$ TC2=0.79e-6 $°C^{-2}$	2.29
Unsilic. N+ poly	990	107e-6/V	TC1=-2.46e-3 $°C^{-1}$ TC2=5.73e-6 $°C^{-2}$	2.5
Unsilic. N+ poly with predoping	110	43e-6/V	TC1=0.19e-3 $°C^{-1}$ TC2=0.38e-6 $°C^{-2}$	4.2
Hipo	6350	-550e-6/V	TC1=-3.14e-3 $°C^{-1}$ TC2=8.30e-6 $°C^{-2}$	3.1
Poly-poly shielded	1575	0e-6/V	TC1=-3.32e-3 $°C^{-1}$ TC2=8.70e-6 $°C^{-2}$	5.0
Thin Film resistor	576	0e-6/V	TC1=-0.019e-3 $°C^{-1}$ TC2=0 e-6 $°C^{-2}$	0.63

Capacitors electrical parameters

Capacitor type	Intrinsic capacitance [nF/mm^2]	Capacitance modulation ($\Delta C/C$) [%]
1.8V poly on silicon	8.15 @ -1.8V	29.5 (-1.8V, 0)
1.8V poly on silicon with Capacitor impl.	8.43 @ 1.8V	10.1 (0, 1.8V) 49.7 (-1.8V, 1.8V)
3.3V poly on silicon	4.67 @ -3.3V	23.0 (-3.3V, 0)
3.3V poly on silicon with Capacitor impl	3.94 @ 3.3V	-5.95 (0, 3.3V) 16.9 (-3.3V, 3.3V)
5V poly-poly	2.67 @ 0V	-1.2 (-5V, 5V)
Interdigitated metal	646 pF/mm^2	
100V metal	123 pF/mm^2	
200V metal	22.4 pF/mm^2	

Thank You